Generate File步骤

Started : "Synthesize - XST".

Running xst...

Command Line: xst -intstyle ise -ifn "F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/topMain.xst" -ofn "F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/topMain.syr"

Reading design: topMain.prj

=========================================================================

\* HDL Compilation \*

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Compiling verilog file "\_rtl/ethmac\_v1\_8/example\_design/physical/rocketio\_wrapper\_gtp\_tile.v" in library work

Compiling verilog file "\_rtl/ethmac\_v1\_8/example\_design/physical/rocketio\_wrapper\_gtp.v" in library work

Module <ROCKETIO\_WRAPPER\_GTP\_TILE> compiled

Compiling verilog file "\_rtl/ethmac\_v1\_8/example\_design/physical/gtp\_dual\_1000X.v" in library work

Module <ROCKETIO\_WRAPPER\_GTP> compiled

Compiling verilog file "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" in library work

Module <GTP\_dual\_1000X> compiled

Compiling verilog file "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/tx\_client\_fifo\_8.v" in library work

Module <ethmac\_v1\_8> compiled

Compiling verilog file "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/rx\_client\_fifo\_8.v" in library work

Module <tx\_client\_fifo\_8> compiled

Compiling verilog file "\_rtl/spi/trunk/rtl/verilog/spi\_shift.v" in library work

Compiling verilog include file "\_rtl/spi/trunk/rtl/verilog/spi\_defines.v"

Compiling verilog include file "\_rtl/spi/trunk/rtl/verilog/timescale.v"

Module <rx\_client\_fifo\_8> compiled

Compiling verilog file "\_rtl/spi/trunk/rtl/verilog/spi\_clgen.v" in library work

Compiling verilog include file "\_rtl/spi/trunk/rtl/verilog/spi\_defines.v"

Compiling verilog include file "\_rtl/spi/trunk/rtl/verilog/timescale.v"

Module <spi\_shift> compiled

Compiling verilog file "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_block.v" in library work

Module <spi\_clgen> compiled

Compiling verilog file "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/eth\_fifo\_8.v" in library work

Module <ethmac\_v1\_8\_block> compiled

Compiling verilog file "\_rtl/spi/trunk/rtl/verilog/spi\_top.v" in library work

Compiling verilog include file "\_rtl/spi/trunk/rtl/verilog/spi\_defines.v"

Compiling verilog include file "\_rtl/spi/trunk/rtl/verilog/timescale.v"

Module <eth\_fifo\_8> compiled

Compiling verilog file "\_rtl/ethmac\_v1\_8/example\_design/rx\_check.v" in library work

Module <spi\_top> compiled

Compiling verilog file "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_locallink.v" in library work

Module <rx\_check> compiled

Compiling verilog file "ipcore\_dir/dualPortRAM.v" in library work

Module <ethmac\_v1\_8\_locallink> compiled

Compiling verilog file "\_rtl/user\_spi\_flash\_ctrl.v" in library work

Module <dualPortRAM> compiled

Compiling verilog file "\_rtl/tx\_control.v" in library work

Module <user\_spi\_flash\_ctrl> compiled

Compiling verilog file "\_rtl/m25pxx\_spi\_flash\_ctrl.v" in library work

Compiling verilog include file "\_rtl/spi\trunk\rtl\verilog\spi\_defines.v"

Module <tx\_control> compiled

Compiling verilog file "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_design.v" in library work

Module <m25pxx\_spi\_flash\_ctrl> compiled

Compiling verilog file "\_rtl/Div\_Ctrl.v" in library work

Module <ethmac\_v1\_8\_design> compiled

Compiling verilog file "topMain.vf" in library work

Module <Div\_Ctrl> compiled

Module <topMain> compiled

No errors in compilation

Analysis of file <"topMain.prj"> succeeded.

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\* Design Hierarchy Analysis \*

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Analyzing hierarchy for module <topMain> in library <work>.

Analyzing hierarchy for module <ethmac\_v1\_8\_design> in library <work>.

Analyzing hierarchy for module <Div\_Ctrl> in library <work> with parameters.

TIM\_PRD = "00000000101111101011110000100000"

TIM\_PULSE = "00000111011100110101100101000000"

TIM\_RST\_FB = "00000000000000011110100001001000"

Analyzing hierarchy for module <user\_spi\_flash\_ctrl> in library <work> with parameters.

st\_falsh\_cmd\_check\_WIP\_0 = "011001"

st\_falsh\_cmd\_check\_WIP\_1 = "011010"

st\_flash\_chk\_is\_on = "001000"

st\_flash\_chk\_is\_on\_1 = "001001"

st\_flash\_cmd\_ADDRH = "010011"

st\_flash\_cmd\_ADDRL = "010101"

st\_flash\_cmd\_ADDRM = "010100"

st\_flash\_cmd\_BE\_0 = "001111"

st\_flash\_cmd\_BE\_1 = "010000"

st\_flash\_cmd\_PP = "010010"

st\_flash\_cmd\_WREN = "010001"

st\_flash\_cmd\_data\_done = "011000"

st\_flash\_cmd\_data\_rd = "010110"

st\_flash\_cmd\_data\_wr = "010111"

st\_flash\_idle = "000000"

st\_flash\_init = "000001"

st\_flash\_rdid\_0 = "001010"

st\_flash\_rdid\_1 = "001011"

st\_flash\_rdid\_2 = "001100"

st\_flash\_rdid\_over = "001101"

st\_flash\_res\_0 = "000010"

st\_flash\_res\_1 = "000011"

st\_flash\_res\_2 = "000100"

st\_flash\_res\_3 = "000101"

st\_flash\_res\_4 = "000110"

st\_flash\_res\_5 = "000111"

st\_flash\_wait\_cmd = "001110"

st\_rx\_config\_data = "01111"

st\_rx\_config\_data\_0 = "01010"

st\_rx\_config\_data\_1 = "01011"

st\_rx\_config\_data\_2 = "01100"

st\_rx\_config\_data\_3 = "01101"

st\_rx\_config\_data\_4 = "01110"

st\_rx\_config\_data\_done = "10000"

st\_rx\_config\_head\_1 = "00111"

st\_rx\_config\_head\_2 = "01000"

st\_rx\_config\_head\_3 = "01001"

st\_rx\_config\_idle = "00000"

st\_rx\_config\_send\_msg = "00010"

st\_rx\_config\_wait\_1 = "00011"

st\_rx\_config\_wait\_2 = "00100"

st\_rx\_config\_wait\_3 = "00101"

st\_rx\_config\_wait\_be\_done = "00001"

st\_rx\_config\_wait\_cmd = "00110"

st\_rx\_config\_wait\_pp = "10001"

st\_rx\_config\_wait\_wip0 = "11111"

st\_wait\_sync\_chk0 = "001"

st\_wait\_sync\_chk1 = "010"

st\_wait\_sync\_chk2 = "011"

st\_wait\_sync\_chk3 = "100"

st\_wait\_sync\_idle = "000"

Analyzing hierarchy for module <tx\_control> in library <work> with parameters.

TX\_DA1 = "0000000000000001"

TX\_DA2 = "0000000000000010"

TX\_DA3 = "0000000000000100"

TX\_DA4 = "0000000000001000"

TX\_DA5 = "0000000000010000"

TX\_DA6 = "0000000000100000"

TX\_DAT = "0100000000000000"

TX\_IDLE = "0000000000000000"

TX\_LEH = "0001000000000000"

TX\_LEL = "0010000000000000"

TX\_SA1 = "0000000001000000"

TX\_SA2 = "0000000010000000"

TX\_SA3 = "0000000100000000"

TX\_SA4 = "0000001000000000"

TX\_SA5 = "0000010000000000"

TX\_SA6 = "0000100000000000"

Analyzing hierarchy for module <m25pxx\_spi\_flash\_ctrl> in library <work> with parameters.

ST\_IDLE = "00000000"

ST\_SPI\_CTRL\_0 = "00000011"

ST\_SPI\_INIT\_DIV = "00000010"

ST\_SPI\_INIT\_SS = "00000001"

ST\_SPI\_PP\_BRANCH = "00111101"

ST\_SPI\_PP\_CTRL\_GO\_ADDH = "00110010"

ST\_SPI\_PP\_CTRL\_GO\_ADDL = "00111000"

ST\_SPI\_PP\_CTRL\_GO\_ADDM = "00110101"

ST\_SPI\_PP\_CTRL\_GO\_CMD = "00101111"

ST\_SPI\_PP\_CTRL\_GO\_DATA = "00111011"

ST\_SPI\_PP\_SS\_CLEAR = "00111110"

ST\_SPI\_PP\_SS\_SET = "00101110"

ST\_SPI\_PP\_TX0\_ADDH = "00110001"

ST\_SPI\_PP\_TX0\_ADDL = "00110111"

ST\_SPI\_PP\_TX0\_ADDM = "00110100"

ST\_SPI\_PP\_TX0\_CMD = "00101101"

ST\_SPI\_PP\_TX0\_DATA = "00111010"

ST\_SPI\_PP\_WAIT\_ADDH = "00110011"

ST\_SPI\_PP\_WAIT\_ADDL = "00111001"

ST\_SPI\_PP\_WAIT\_ADDM = "00110110"

ST\_SPI\_PP\_WAIT\_CMD = "00110000"

ST\_SPI\_PP\_WAIT\_DATA = "00111100"

ST\_SPI\_PP\_WREN\_CTRL\_GO = "00101010"

ST\_SPI\_PP\_WREN\_SS\_CLEAR = "00101100"

ST\_SPI\_PP\_WREN\_SS\_SET = "00101001"

ST\_SPI\_PP\_WREN\_TX0 = "00101000"

ST\_SPI\_PP\_WREN\_WAIT = "00101011"

ST\_SPI\_RDID\_CTRL\_GO = "00000110"

ST\_SPI\_RDID\_RD\_DUMMY = "00001000"

ST\_SPI\_RDID\_SS\_CLEAR = "00010010"

ST\_SPI\_RDID\_SS\_SET\_RDID = "00000101"

ST\_SPI\_RDID\_TXCMD = "00000100"

ST\_SPI\_RDID\_TX\_DUMMY1 = "00001001"

ST\_SPI\_RDID\_TX\_DUMMY2 = "00001100"

ST\_SPI\_RDID\_TX\_DUMMY3 = "00001111"

ST\_SPI\_RDID\_WAIT0 = "00000111"

ST\_SPI\_RDID\_WAIT1 = "00001010"

ST\_SPI\_RDID\_WAIT2 = "00001101"

ST\_SPI\_RDID\_WAIT3 = "00010000"

ST\_SPI\_RDID\_manuID = "00001011"

ST\_SPI\_RDID\_memType = "00001110"

ST\_SPI\_RDID\_menCap = "00010001"

ST\_SPI\_RDSR\_BRANCH = "00100110"

ST\_SPI\_RDSR\_CTRL\_GO = "00100000"

ST\_SPI\_RDSR\_CTRL\_GO\_NOP = "00100011"

ST\_SPI\_RDSR\_READ = "00100101"

ST\_SPI\_RDSR\_SS\_CLEAR = "00100111"

ST\_SPI\_RDSR\_SS\_SET = "00011111"

ST\_SPI\_RDSR\_TX0 = "00011110"

ST\_SPI\_RDSR\_TX0\_NOP = "00100010"

ST\_SPI\_RDSR\_WAIT = "00100001"

ST\_SPI\_RDSR\_WAIT\_1 = "00100100"

ST\_SPI\_RD\_BRANCH = "01001111"

ST\_SPI\_RD\_CTRL\_GO\_ADDH = "01000100"

ST\_SPI\_RD\_CTRL\_GO\_ADDL = "01001010"

ST\_SPI\_RD\_CTRL\_GO\_ADDM = "01000111"

ST\_SPI\_RD\_CTRL\_GO\_CMD = "01000001"

ST\_SPI\_RD\_CTRL\_GO\_DATA = "01001101"

ST\_SPI\_RD\_SS\_CLEAR = "01010000"

ST\_SPI\_RD\_SS\_SET = "01000000"

ST\_SPI\_RD\_TX0\_ADDH = "01000011"

ST\_SPI\_RD\_TX0\_ADDL = "01001001"

ST\_SPI\_RD\_TX0\_ADDM = "01000110"

ST\_SPI\_RD\_TX0\_CMD = "00111111"

ST\_SPI\_RD\_TX0\_DATA = "01001100"

ST\_SPI\_RD\_WAIT\_ADDH = "01000101"

ST\_SPI\_RD\_WAIT\_ADDL = "01001011"

ST\_SPI\_RD\_WAIT\_ADDM = "01001000"

ST\_SPI\_RD\_WAIT\_CMD = "01000010"

ST\_SPI\_RD\_WAIT\_DATA = "01001110"

ST\_SPI\_SE\_CTRL\_GO = "00011011"

ST\_SPI\_SE\_SS\_CLEAR = "00011101"

ST\_SPI\_SE\_SS\_SET = "00011010"

ST\_SPI\_SE\_TX0 = "00011001"

ST\_SPI\_SE\_WAIT = "00011100"

ST\_SPI\_WAIT = "00010011"

ST\_SPI\_WREN\_CTRL\_GO = "00010110"

ST\_SPI\_WREN\_SS\_CLEAR = "00011000"

ST\_SPI\_WREN\_SS\_SET = "00010101"

ST\_SPI\_WREN\_TX0 = "00010100"

ST\_SPI\_WREN\_WAIT = "00010111"

Analyzing hierarchy for module <ethmac\_v1\_8\_locallink> in library <work>.

Analyzing hierarchy for module <rx\_check> in library <work> with parameters.

ST\_DATA = "00010"

ST\_END = "00100"

ST\_IDLE = "00000"

ST\_LAST = "00011"

ST\_WAIT = "00001"

Analyzing hierarchy for module <spi\_top> in library <work> with parameters.

Tp = "00000000000000000000000000000001"

Analyzing hierarchy for module <ethmac\_v1\_8\_block> in library <work>.

Analyzing hierarchy for module <eth\_fifo\_8> in library <work> with parameters.

FULL\_DUPLEX\_ONLY = "00000000000000000000000000000000"

Analyzing hierarchy for module <eth\_fifo\_8> in library <work> with parameters.

FULL\_DUPLEX\_ONLY = "00000000000000000000000000000000"

Analyzing hierarchy for module <spi\_clgen> in library <work> with parameters.

Tp = "00000000000000000000000000000001"

Analyzing hierarchy for module <spi\_shift> in library <work> with parameters.

Tp = "00000000000000000000000000000001"

Analyzing hierarchy for module <GTP\_dual\_1000X> in library <work>.

Analyzing hierarchy for module <ethmac\_v1\_8> in library <work>.

Analyzing hierarchy for module <tx\_client\_fifo\_8> in library <work> with parameters.

DATA\_s = "01"

DROP\_s = "0111"

EOF\_s = "10"

FRAME\_s = "0110"

FULL\_DUPLEX\_ONLY = "00000000000000000000000000000000"

IDLE\_s = "0000"

OVFLOW\_s = "11"

QUEUE1\_s = "0001"

QUEUE2\_s = "0010"

QUEUE3\_s = "0011"

QUEUE\_ACK\_s = "0100"

RETRANSMIT\_s = "1000"

WAIT\_ACK\_s = "0101"

WAIT\_s = "00"

Analyzing hierarchy for module <rx\_client\_fifo\_8> in library <work> with parameters.

BF\_s = "100"

DATA\_s = "110"

END\_s = "010"

EOF\_s = "111"

FRAME\_s = "001"

GF\_s = "011"

IDLE\_s = "000"

OVFLOW\_s = "101"

QUEUE1\_s = "001"

QUEUE2\_s = "010"

QUEUE3\_s = "011"

QUEUE\_SOF\_s = "100"

SOF\_s = "101"

WAIT\_s = "000"

Analyzing hierarchy for module <tx\_client\_fifo\_8> in library <work> with parameters.

DATA\_s = "01"

DROP\_s = "0111"

EOF\_s = "10"

FRAME\_s = "0110"

FULL\_DUPLEX\_ONLY = "00000000000000000000000000000000"

IDLE\_s = "0000"

OVFLOW\_s = "11"

QUEUE1\_s = "0001"

QUEUE2\_s = "0010"

QUEUE3\_s = "0011"

QUEUE\_ACK\_s = "0100"

RETRANSMIT\_s = "1000"

WAIT\_ACK\_s = "0101"

WAIT\_s = "00"

Analyzing hierarchy for module <rx\_client\_fifo\_8> in library <work> with parameters.

BF\_s = "100"

DATA\_s = "110"

END\_s = "010"

EOF\_s = "111"

FRAME\_s = "001"

GF\_s = "011"

IDLE\_s = "000"

OVFLOW\_s = "101"

QUEUE1\_s = "001"

QUEUE2\_s = "010"

QUEUE3\_s = "011"

QUEUE\_SOF\_s = "100"

SOF\_s = "101"

WAIT\_s = "000"

Analyzing hierarchy for module <ROCKETIO\_WRAPPER\_GTP> in library <work> with parameters.

WRAPPER\_SIM\_GTPRESET\_SPEEDUP = "00000000000000000000000000000001"

WRAPPER\_SIM\_PLL\_PERDIV2 = "110010000"

Analyzing hierarchy for module <ROCKETIO\_WRAPPER\_GTP\_TILE> in library <work> with parameters.

TILE\_CHAN\_BOND\_LEVEL\_0 = "00000000000000000000000000000000"

TILE\_CHAN\_BOND\_LEVEL\_1 = "00000000000000000000000000000000"

TILE\_CHAN\_BOND\_MODE\_0 = "OFF"

TILE\_CHAN\_BOND\_MODE\_1 = "OFF"

TILE\_SIM\_GTPRESET\_SPEEDUP = "00000000000000000000000000000001"

TILE\_SIM\_PLL\_PERDIV2 = "110010000"

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/tx\_client\_fifo\_8.v" line 1242: attribute on instance <WRITE\_MODE\_A> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/tx\_client\_fifo\_8.v" line 1242: attribute on instance <WRITE\_MODE\_B> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/tx\_client\_fifo\_8.v" line 1265: attribute on instance <WRITE\_MODE\_A> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/tx\_client\_fifo\_8.v" line 1265: attribute on instance <WRITE\_MODE\_B> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_1000BASEX\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_ADDRFILTER\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_BYTEPHY> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_CONFIGVEC\_79> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_DCRBASEADDR> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_GTLOOPBACK> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_HOST\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_LINKTIMERVAL> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_LTCHECK\_DISABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_MDIO\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_PAUSEADDR> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_PHYINITAUTONEG\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_PHYISOLATE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_PHYLOOPBACKMSB> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_PHYPOWERDOWN> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_PHYRESET> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_RGMII\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_RX16BITCLIENT\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_RXFLOWCTRL\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_RXHALFDUPLEX> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_RXINBANDFCS\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_RXJUMBOFRAME\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_RXRESET> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_RXVLAN\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_RX\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_SGMII\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_SPEED\_LSB> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_SPEED\_MSB> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_TX16BITCLIENT\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_TXFLOWCTRL\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_TXHALFDUPLEX> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

Started : "Launching Custom Editor to edit ethmac\_v1\_8.v".

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_TXIFGADJUST\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_TXINBANDFCS\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_TXJUMBOFRAME\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_TXRESET> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_TXVLAN\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_TX\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_UNICASTADDR> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_UNIDIRECTION\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC0\_USECLKEN> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_1000BASEX\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_ADDRFILTER\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_BYTEPHY> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_CONFIGVEC\_79> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_DCRBASEADDR> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_GTLOOPBACK> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_HOST\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_LINKTIMERVAL> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_LTCHECK\_DISABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_MDIO\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_PAUSEADDR> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_PHYINITAUTONEG\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_PHYISOLATE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_PHYLOOPBACKMSB> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_PHYPOWERDOWN> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_PHYRESET> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_RGMII\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_RX16BITCLIENT\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_RXFLOWCTRL\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_RXHALFDUPLEX> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_RXINBANDFCS\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_RXJUMBOFRAME\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_RXRESET> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_RXVLAN\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_RX\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_SGMII\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_SPEED\_LSB> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_SPEED\_MSB> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_TX16BITCLIENT\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_TXFLOWCTRL\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_TXHALFDUPLEX> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_TXIFGADJUST\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_TXINBANDFCS\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_TXJUMBOFRAME\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_TXRESET> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_TXVLAN\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_TX\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_UNICASTADDR> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_UNIDIRECTION\_ENABLE> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

WARNING:Xst:2591 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 418: attribute on instance <EMAC1\_USECLKEN> overrides generic/parameter on entity. It is possible that simulator will not take this attribute into account.

=========================================================================

\* HDL Analysis \*

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Analyzing top module <topMain>.

WARNING:Xst:852 - "topMain.vf" line 87: Unconnected input port 'CLK125\_DS' of instance 'XLXI\_1' is tied to GND.

WARNING:Xst:852 - "topMain.vf" line 87: Unconnected input port 'RX\_LL\_DST\_RDY\_N\_1' of instance 'XLXI\_1' is tied to GND.

Module <topMain> is correct for synthesis.

Set user-defined property "BANDWIDTH = OPTIMIZED" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKFBOUT\_MULT = 4" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKFBOUT\_PHASE = 0.000000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKIN\_PERIOD = 8.000000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT0\_DIVIDE = 20" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT0\_DUTY\_CYCLE = 0.500000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT0\_PHASE = 0.000000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT1\_DIVIDE = 1" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT1\_DUTY\_CYCLE = 0.500000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT1\_PHASE = 0.000000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT2\_DIVIDE = 1" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT2\_DUTY\_CYCLE = 0.500000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT2\_PHASE = 0.000000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT3\_DIVIDE = 1" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT3\_DUTY\_CYCLE = 0.500000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT3\_PHASE = 0.000000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT4\_DIVIDE = 1" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT4\_DUTY\_CYCLE = 0.500000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT4\_PHASE = 0.000000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT5\_DIVIDE = 1" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT5\_DUTY\_CYCLE = 0.500000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLKOUT5\_PHASE = 0.000000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "CLK\_FEEDBACK = CLKFBOUT" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "COMPENSATION = SYSTEM\_SYNCHRONOUS" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "DIVCLK\_DIVIDE = 1" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "REF\_JITTER = 0.100000" for instance <XLXI\_9> in unit <topMain>.

Set user-defined property "RESET\_ON\_LOSS\_OF\_LOCK = FALSE" for instance <XLXI\_9> in unit <topMain>.

Analyzing module <ethmac\_v1\_8\_design> in library <work>.

WARNING:Xst:1464 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_design.v" line 560: Exactly equal expression will be synthesized as an equal expression, simulation mismatch is possible.

WARNING:Xst:1464 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_design.v" line 565: Exactly equal expression will be synthesized as an equal expression, simulation mismatch is possible.

WARNING:Xst:1464 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_design.v" line 579: Exactly equal expression will be synthesized as an equal expression, simulation mismatch is possible.

WARNING:Xst:1464 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_design.v" line 584: Exactly equal expression will be synthesized as an equal expression, simulation mismatch is possible.

WARNING:Xst:852 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_design.v" line 383: Unconnected input port 'CLIENTEMAC0PAUSEREQ' of instance 'v5\_emac\_ll' is tied to GND.

WARNING:Xst:852 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_design.v" line 383: Unconnected input port 'CLIENTEMAC1PAUSEREQ' of instance 'v5\_emac\_ll' is tied to GND.

WARNING:Xst:852 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_design.v" line 383: Unconnected input port 'CLIENTEMAC1PAUSEVAL' of instance 'v5\_emac\_ll' is tied to GND.

Module <ethmac\_v1\_8\_design> is correct for synthesis.

Set user-defined property "CAPACITANCE = DONT\_CARE" for instance <clkingen> in unit <ethmac\_v1\_8\_design>.

Set user-defined property "DIFF\_TERM = FALSE" for instance <clkingen> in unit <ethmac\_v1\_8\_design>.

Set user-defined property "IBUF\_DELAY\_VALUE = 0" for instance <clkingen> in unit <ethmac\_v1\_8\_design>.

Set user-defined property "IBUF\_LOW\_PWR = TRUE" for instance <clkingen> in unit <ethmac\_v1\_8\_design>.

Set user-defined property "IFD\_DELAY\_VALUE = AUTO" for instance <clkingen> in unit <ethmac\_v1\_8\_design>.

Set user-defined property "IOSTANDARD = DEFAULT" for instance <clkingen> in unit <ethmac\_v1\_8\_design>.

Set property "buffer\_type = none" for signal <host\_clk\_i>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <reset\_r>.

Analyzing module <ethmac\_v1\_8\_locallink> in library <work>.

WARNING:Xst:1464 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_locallink.v" line 595: Exactly equal expression will be synthesized as an equal expression, simulation mismatch is possible.

WARNING:Xst:1464 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_locallink.v" line 613: Exactly equal expression will be synthesized as an equal expression, simulation mismatch is possible.

WARNING:Xst:1464 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_locallink.v" line 711: Exactly equal expression will be synthesized as an equal expression, simulation mismatch is possible.

WARNING:Xst:1464 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_locallink.v" line 730: Exactly equal expression will be synthesized as an equal expression, simulation mismatch is possible.

Module <ethmac\_v1\_8\_locallink> is correct for synthesis.

Set user-defined property "KEEP = true" for signal <tx\_data\_1\_i>.

Set user-defined property "KEEP = true" for signal <tx\_ack\_0\_i>.

Set user-defined property "KEEP = true" for signal <tx\_ack\_1\_i>.

Set user-defined property "KEEP = true" for signal <rx\_data\_valid\_0\_i>.

Set user-defined property "KEEP = true" for signal <rx\_data\_valid\_1\_i>.

Set user-defined property "KEEP = true" for signal <rx\_data\_0\_i>.

Set user-defined property "KEEP = true" for signal <tx\_data\_valid\_0\_i>.

Set user-defined property "KEEP = true" for signal <rx\_data\_1\_i>.

Set user-defined property "KEEP = true" for signal <tx\_data\_valid\_1\_i>.

Set user-defined property "KEEP = true" for signal <tx\_data\_0\_i>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <tx\_pre\_reset\_0\_i>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <rx\_pre\_reset\_0\_i>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <tx\_pre\_reset\_1\_i>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <rx\_pre\_reset\_1\_i>.

Analyzing module <ethmac\_v1\_8\_block> in library <work>.

Module <ethmac\_v1\_8\_block> is correct for synthesis.

Set user-defined property "ASYNC\_REG = TRUE" for signal <reset\_r>.

Analyzing module <GTP\_dual\_1000X> in library <work>.

Module <GTP\_dual\_1000X> is correct for synthesis.

Analyzing module <ROCKETIO\_WRAPPER\_GTP> in library <work>.

WRAPPER\_SIM\_GTPRESET\_SPEEDUP = 32'sb00000000000000000000000000000001

WRAPPER\_SIM\_PLL\_PERDIV2 = 9'b110010000

Module <ROCKETIO\_WRAPPER\_GTP> is correct for synthesis.

Analyzing module <ROCKETIO\_WRAPPER\_GTP\_TILE> in library <work>.

TILE\_CHAN\_BOND\_LEVEL\_0 = 32'sb00000000000000000000000000000000

TILE\_CHAN\_BOND\_LEVEL\_1 = 32'sb00000000000000000000000000000000

TILE\_CHAN\_BOND\_MODE\_0 = "OFF"

TILE\_CHAN\_BOND\_MODE\_1 = "OFF"

TILE\_SIM\_GTPRESET\_SPEEDUP = 32'sb00000000000000000000000000000001

TILE\_SIM\_PLL\_PERDIV2 = 9'b110010000

Module <ROCKETIO\_WRAPPER\_GTP\_TILE> is correct for synthesis.

Set user-defined property "AC\_CAP\_DIS\_0 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "AC\_CAP\_DIS\_1 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "ALIGN\_COMMA\_WORD\_0 = 1" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "ALIGN\_COMMA\_WORD\_1 = 1" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_1\_MAX\_SKEW\_0 = 7" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_1\_MAX\_SKEW\_1 = 7" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_2\_MAX\_SKEW\_0 = 7" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_2\_MAX\_SKEW\_1 = 7" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_LEVEL\_0 = 0" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_LEVEL\_1 = 0" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_MODE\_0 = OFF" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_MODE\_1 = OFF" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_1\_1\_0 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_1\_1\_1 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_1\_2\_0 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_1\_2\_1 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_1\_3\_0 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_1\_3\_1 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_1\_4\_0 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_1\_4\_1 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_1\_ENABLE\_0 = 0000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_1\_ENABLE\_1 = 0000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_2\_1\_0 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_2\_1\_1 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_2\_2\_0 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_2\_2\_1 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_2\_3\_0 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_2\_3\_1 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_2\_4\_0 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_2\_4\_1 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_2\_ENABLE\_0 = 0000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_2\_ENABLE\_1 = 0000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_2\_USE\_0 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_2\_USE\_1 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_LEN\_0 = 1" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CHAN\_BOND\_SEQ\_LEN\_1 = 1" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK25\_DIVIDER = 5" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLKINDC\_B = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_CORRECT\_USE\_0 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_CORRECT\_USE\_1 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_ADJ\_LEN\_0 = 2" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_ADJ\_LEN\_1 = 2" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_DET\_LEN\_0 = 2" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_DET\_LEN\_1 = 2" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_INSERT\_IDLE\_FLAG\_0 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_INSERT\_IDLE\_FLAG\_1 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_KEEP\_IDLE\_0 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_KEEP\_IDLE\_1 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_MAX\_LAT\_0 = 18" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_MAX\_LAT\_1 = 18" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_MIN\_LAT\_0 = 16" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_MIN\_LAT\_1 = 16" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_PRECEDENCE\_0 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_PRECEDENCE\_1 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_REPEAT\_WAIT\_0 = 0" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_REPEAT\_WAIT\_1 = 0" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_1\_1\_0 = 0110111100" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_1\_1\_1 = 0110111100" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_1\_2\_0 = 0001010000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_1\_2\_1 = 0001010000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_1\_3\_0 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_1\_3\_1 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_1\_4\_0 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_1\_4\_1 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_1\_ENABLE\_0 = 0011" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_1\_ENABLE\_1 = 0011" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_2\_1\_0 = 0110111100" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_2\_1\_1 = 0110111100" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_2\_2\_0 = 0010110101" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_2\_2\_1 = 0010110101" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_2\_3\_0 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_2\_3\_1 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_2\_4\_0 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_2\_4\_1 = 0000000000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_2\_ENABLE\_0 = 0011" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_2\_ENABLE\_1 = 0011" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_2\_USE\_0 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "CLK\_COR\_SEQ\_2\_USE\_1 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "COMMA\_10B\_ENABLE\_0 = 0001111111" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "COMMA\_10B\_ENABLE\_1 = 0001111111" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "COMMA\_DOUBLE\_0 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "COMMA\_DOUBLE\_1 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "COM\_BURST\_VAL\_0 = 1111" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "COM\_BURST\_VAL\_1 = 1111" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "DEC\_MCOMMA\_DETECT\_0 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "DEC\_MCOMMA\_DETECT\_1 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "DEC\_PCOMMA\_DETECT\_0 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "DEC\_PCOMMA\_DETECT\_1 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "DEC\_VALID\_COMMA\_ONLY\_0 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "DEC\_VALID\_COMMA\_ONLY\_1 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "MCOMMA\_10B\_VALUE\_0 = 1010000011" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "MCOMMA\_10B\_VALUE\_1 = 1010000011" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "MCOMMA\_DETECT\_0 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "MCOMMA\_DETECT\_1 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "OOBDETECT\_THRESHOLD\_0 = 001" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "OOBDETECT\_THRESHOLD\_1 = 001" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "OOB\_CLK\_DIVIDER = 4" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "OVERSAMPLE\_MODE = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PCI\_EXPRESS\_MODE\_0 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PCI\_EXPRESS\_MODE\_1 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PCOMMA\_10B\_VALUE\_0 = 0101111100" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PCOMMA\_10B\_VALUE\_1 = 0101111100" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PCOMMA\_DETECT\_0 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PCOMMA\_DETECT\_1 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PCS\_COM\_CFG = 1680A0E" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PLL\_DIVSEL\_FB = 2" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PLL\_DIVSEL\_REF = 1" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PLL\_RXDIVSEL\_OUT\_0 = 2" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PLL\_RXDIVSEL\_OUT\_1 = 2" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PLL\_SATA\_0 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PLL\_SATA\_1 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PLL\_TXDIVSEL\_COMM\_OUT = 1" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PLL\_TXDIVSEL\_OUT\_0 = 2" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PLL\_TXDIVSEL\_OUT\_1 = 2" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PMA\_CDR\_SCAN\_0 = 6C07640" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PMA\_CDR\_SCAN\_1 = 6C07640" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PMA\_RX\_CFG\_0 = 09F0088" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PMA\_RX\_CFG\_1 = 09F0088" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PRBS\_ERR\_THRESHOLD\_0 = 00000001" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "PRBS\_ERR\_THRESHOLD\_1 = 00000001" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RCV\_TERM\_GND\_0 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RCV\_TERM\_GND\_1 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RCV\_TERM\_MID\_0 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RCV\_TERM\_MID\_1 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RCV\_TERM\_VTTRX\_0 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RCV\_TERM\_VTTRX\_1 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_BUFFER\_USE\_0 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_BUFFER\_USE\_1 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_DECODE\_SEQ\_MATCH\_0 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_DECODE\_SEQ\_MATCH\_1 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_LOSS\_OF\_SYNC\_FSM\_0 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_LOSS\_OF\_SYNC\_FSM\_1 = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_LOS\_INVALID\_INCR\_0 = 8" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_LOS\_INVALID\_INCR\_1 = 8" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_LOS\_THRESHOLD\_0 = 128" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_LOS\_THRESHOLD\_1 = 128" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_SLIDE\_MODE\_0 = PCS" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_SLIDE\_MODE\_1 = PCS" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_STATUS\_FMT\_0 = PCIE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_STATUS\_FMT\_1 = PCIE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_XCLK\_SEL\_0 = RXREC" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "RX\_XCLK\_SEL\_1 = RXREC" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_BURST\_VAL\_0 = 100" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_BURST\_VAL\_1 = 100" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_IDLE\_VAL\_0 = 100" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_IDLE\_VAL\_1 = 100" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_MAX\_BURST\_0 = 9" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_MAX\_BURST\_1 = 9" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_MAX\_INIT\_0 = 27" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_MAX\_INIT\_1 = 27" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_MAX\_WAKE\_0 = 9" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_MAX\_WAKE\_1 = 9" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_MIN\_BURST\_0 = 5" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_MIN\_BURST\_1 = 5" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_MIN\_INIT\_0 = 15" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_MIN\_INIT\_1 = 15" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_MIN\_WAKE\_0 = 5" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SATA\_MIN\_WAKE\_1 = 5" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SIM\_GTPRESET\_SPEEDUP = 1" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SIM\_MODE = FAST" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SIM\_PLL\_PERDIV2 = 190" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SIM\_RECEIVER\_DETECT\_PASS0 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "SIM\_RECEIVER\_DETECT\_PASS1 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TERMINATION\_CTRL = 10100" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TERMINATION\_IMP\_0 = 50" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TERMINATION\_IMP\_1 = 50" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TERMINATION\_OVRD = FALSE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TRANS\_TIME\_FROM\_P2\_0 = 003C" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TRANS\_TIME\_FROM\_P2\_1 = 003C" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TRANS\_TIME\_NON\_P2\_0 = 0019" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TRANS\_TIME\_NON\_P2\_1 = 0019" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TRANS\_TIME\_TO\_P2\_0 = 0064" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TRANS\_TIME\_TO\_P2\_1 = 0064" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TXRX\_INVERT\_0 = 00000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TXRX\_INVERT\_1 = 00000" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TX\_BUFFER\_USE\_0 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TX\_BUFFER\_USE\_1 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TX\_DIFF\_BOOST\_0 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TX\_DIFF\_BOOST\_1 = TRUE" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TX\_SYNC\_FILTERB = 1" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TX\_XCLK\_SEL\_0 = TXOUT" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Set user-defined property "TX\_XCLK\_SEL\_1 = TXOUT" for instance <gtp\_dual\_i> in unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Analyzing module <ethmac\_v1\_8> in library <work>.

WARNING:Xst:916 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 407: Delay is ignored for synthesis.

WARNING:Xst:916 - "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v" line 411: Delay is ignored for synthesis.

Module <ethmac\_v1\_8> is correct for synthesis.

Set user-defined property "EMAC0\_1000BASEX\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_ADDRFILTER\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_BYTEPHY = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_CONFIGVEC\_79 = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_DCRBASEADDR = 8'h00" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_GTLOOPBACK = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_HOST\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_LINKTIMERVAL = 9'h13D" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_LTCHECK\_DISABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_MDIO\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_PAUSEADDR = 48'h9D\_1b\_05\_19\_22\_00" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_PHYINITAUTONEG\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_PHYISOLATE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_PHYLOOPBACKMSB = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_PHYPOWERDOWN = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_PHYRESET = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_RGMII\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_RX16BITCLIENT\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_RXFLOWCTRL\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_RXHALFDUPLEX = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_RXINBANDFCS\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_RXJUMBOFRAME\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_RXRESET = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_RXVLAN\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_RX\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_SGMII\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_SPEED\_LSB = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_SPEED\_MSB = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_TX16BITCLIENT\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_TXFLOWCTRL\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_TXHALFDUPLEX = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_TXIFGADJUST\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_TXINBANDFCS\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_TXJUMBOFRAME\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_TXRESET = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_TXVLAN\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_TX\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_UNICASTADDR = 48'h9D\_1b\_05\_19\_22\_00" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_UNIDIRECTION\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC0\_USECLKEN = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_1000BASEX\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_ADDRFILTER\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_BYTEPHY = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_CONFIGVEC\_79 = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_DCRBASEADDR = 8'h00" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_GTLOOPBACK = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_HOST\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_LINKTIMERVAL = 9'h13D" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_LTCHECK\_DISABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_MDIO\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_PAUSEADDR = 48'h9D\_1b\_05\_19\_22\_00" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_PHYINITAUTONEG\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_PHYISOLATE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_PHYLOOPBACKMSB = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_PHYPOWERDOWN = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_PHYRESET = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_RGMII\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_RX16BITCLIENT\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_RXFLOWCTRL\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_RXHALFDUPLEX = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_RXINBANDFCS\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_RXJUMBOFRAME\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_RXRESET = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_RXVLAN\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_RX\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_SGMII\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_SPEED\_LSB = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_SPEED\_MSB = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_TX16BITCLIENT\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_TXFLOWCTRL\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_TXHALFDUPLEX = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_TXIFGADJUST\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_TXINBANDFCS\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_TXJUMBOFRAME\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_TXRESET = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_TXVLAN\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_TX\_ENABLE = TRUE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_UNICASTADDR = 48'h9D\_1b\_05\_19\_22\_00" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_UNIDIRECTION\_ENABLE = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Set user-defined property "EMAC1\_USECLKEN = FALSE" for instance <v5\_emac> in unit <ethmac\_v1\_8>.

Analyzing module <eth\_fifo\_8.1> in library <work>.

FULL\_DUPLEX\_ONLY = 32'sb00000000000000000000000000000000

Module <eth\_fifo\_8.1> is correct for synthesis.

Analyzing module <tx\_client\_fifo\_8.1> in library <work>.

DATA\_s = 2'b01

DROP\_s = 4'b0111

EOF\_s = 2'b10

FRAME\_s = 4'b0110

FULL\_DUPLEX\_ONLY = 32'sb00000000000000000000000000000000

IDLE\_s = 4'b0000

OVFLOW\_s = 2'b11

QUEUE1\_s = 4'b0001

QUEUE2\_s = 4'b0010

QUEUE3\_s = 4'b0011

QUEUE\_ACK\_s = 4'b0100

RETRANSMIT\_s = 4'b1000

WAIT\_ACK\_s = 4'b0101

WAIT\_s = 2'b00

Module <tx\_client\_fifo\_8.1> is correct for synthesis.

Set user-defined property "INITP\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_08 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_09 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_10 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_11 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_12 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_13 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_14 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_15 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_16 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_17 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_18 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_19 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_20 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_21 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_22 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_23 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_24 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_25 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_26 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_27 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_28 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_29 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_30 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_31 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_32 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_33 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_34 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_35 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_36 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_37 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_38 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_39 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_A = 000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_B = 000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "SIM\_COLLISION\_CHECK = ALL" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "SRVAL\_A = 000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "SRVAL\_B = 000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "WRITE\_MODE\_A = READ\_FIRST" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "WRITE\_MODE\_B = READ\_FIRST" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_08 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_09 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_10 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_11 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_12 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_13 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_14 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_15 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_16 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_17 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_18 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_19 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_20 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_21 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_22 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_23 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_24 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_25 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_26 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_27 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_28 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_29 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_30 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_31 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_32 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_33 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_34 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_35 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_36 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_37 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_38 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_39 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_A = 000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_B = 000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "SIM\_COLLISION\_CHECK = ALL" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "SRVAL\_A = 000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "SRVAL\_B = 000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "WRITE\_MODE\_A = READ\_FIRST" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "WRITE\_MODE\_B = READ\_FIRST" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.1>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <wr\_txfer\_tog>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <wr\_tran\_frame\_tog>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <frame\_in\_fifo\_sync>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <wr\_rd\_addr>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <wr\_retran\_frame\_tog>.

Analyzing module <rx\_client\_fifo\_8.1> in library <work>.

BF\_s = 3'b100

DATA\_s = 3'b110

END\_s = 3'b010

EOF\_s = 3'b111

FRAME\_s = 3'b001

GF\_s = 3'b011

IDLE\_s = 3'b000

OVFLOW\_s = 3'b101

QUEUE1\_s = 3'b001

QUEUE2\_s = 3'b010

QUEUE3\_s = 3'b011

QUEUE\_SOF\_s = 3'b100

SOF\_s = 3'b101

WAIT\_s = 3'b000

WARNING:Xst:905 - "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/rx\_client\_fifo\_8.v" line 307: One or more signals are missing in the sensitivity list of always block. To enable synthesis of FPGA/CPLD hardware, XST will assume that all necessary signals are present in the sensitivity list. Please note that the result of the synthesis may differ from the initial design specification. The missing signals are:

<rd\_valid\_pipe>

Calling function <bin\_to\_gray>.

Calling function <gray\_to\_bin>.

Module <rx\_client\_fifo\_8.1> is correct for synthesis.

Set user-defined property "INITP\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_08 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_09 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_10 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_11 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_12 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_13 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_14 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_15 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_16 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_17 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_18 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_19 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_20 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_21 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_22 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_23 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_24 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_25 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_26 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_27 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_28 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_29 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_30 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_31 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_32 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_33 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_34 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_35 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_36 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_37 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_38 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_39 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_A = 000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_B = 000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "SIM\_COLLISION\_CHECK = ALL" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "SRVAL\_A = 000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "SRVAL\_B = 000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "WRITE\_MODE\_A = READ\_FIRST" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "WRITE\_MODE\_B = READ\_FIRST" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INITP\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_08 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_09 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_0F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_10 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_11 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_12 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_13 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_14 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_15 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_16 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_17 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_18 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_19 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_1F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_20 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_21 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_22 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_23 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_24 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_25 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_26 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_27 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_28 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_29 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_2F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_30 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_31 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_32 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_33 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_34 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_35 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_36 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_37 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_38 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_39 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_3F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_A = 000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "INIT\_B = 000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "SIM\_COLLISION\_CHECK = ALL" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "SRVAL\_A = 000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "SRVAL\_B = 000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "WRITE\_MODE\_A = READ\_FIRST" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "WRITE\_MODE\_B = READ\_FIRST" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.1>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <wr\_rd\_addr\_gray\_sync>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <rd\_store\_frame\_tog>.

Analyzing module <eth\_fifo\_8.2> in library <work>.

FULL\_DUPLEX\_ONLY = 32'sb00000000000000000000000000000000

Module <eth\_fifo\_8.2> is correct for synthesis.

Analyzing module <tx\_client\_fifo\_8.2> in library <work>.

DATA\_s = 2'b01

DROP\_s = 4'b0111

EOF\_s = 2'b10

FRAME\_s = 4'b0110

FULL\_DUPLEX\_ONLY = 32'sb00000000000000000000000000000000

IDLE\_s = 4'b0000

OVFLOW\_s = 2'b11

QUEUE1\_s = 4'b0001

QUEUE2\_s = 4'b0010

QUEUE3\_s = 4'b0011

QUEUE\_ACK\_s = 4'b0100

RETRANSMIT\_s = 4'b1000

WAIT\_ACK\_s = 4'b0101

WAIT\_s = 2'b00

Module <tx\_client\_fifo\_8.2> is correct for synthesis.

Set user-defined property "INITP\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_08 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_09 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_10 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_11 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_12 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_19 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_1A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_1B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_1C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_1F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_20 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_2A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_2F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_30 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_A = 000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_B = 000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "SIM\_COLLISION\_CHECK = ALL" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "SRVAL\_A = 000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "SRVAL\_B = 000000000" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "WRITE\_MODE\_A = READ\_FIRST" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "WRITE\_MODE\_B = READ\_FIRST" for instance <ramgen\_l> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_09 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_30 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_3F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_A = 000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_B = 000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "SIM\_COLLISION\_CHECK = ALL" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "SRVAL\_A = 000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "SRVAL\_B = 000000000" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "WRITE\_MODE\_A = READ\_FIRST" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "WRITE\_MODE\_B = READ\_FIRST" for instance <ramgen\_u> in unit <tx\_client\_fifo\_8.2>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <wr\_txfer\_tog>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <wr\_tran\_frame\_tog>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <frame\_in\_fifo\_sync>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <wr\_rd\_addr>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <wr\_retran\_frame\_tog>.

Analyzing module <rx\_client\_fifo\_8.2> in library <work>.

BF\_s = 3'b100

DATA\_s = 3'b110

END\_s = 3'b010

EOF\_s = 3'b111

FRAME\_s = 3'b001

GF\_s = 3'b011

IDLE\_s = 3'b000

OVFLOW\_s = 3'b101

QUEUE1\_s = 3'b001

QUEUE2\_s = 3'b010

QUEUE3\_s = 3'b011

QUEUE\_SOF\_s = 3'b100

SOF\_s = 3'b101

WAIT\_s = 3'b000

WARNING:Xst:905 - "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/rx\_client\_fifo\_8.v" line 307: One or more signals are missing in the sensitivity list of always block. To enable synthesis of FPGA/CPLD hardware, XST will assume that all necessary signals are present in the sensitivity list. Please note that the result of the synthesis may differ from the initial design specification. The missing signals are:

<rd\_valid\_pipe>

Calling function <bin\_to\_gray>.

Calling function <gray\_to\_bin>.

Module <rx\_client\_fifo\_8.2> is correct for synthesis.

Set user-defined property "INITP\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_09 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_0C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_0F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_30 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

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Set user-defined property "INIT\_3D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_3E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_3F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_A = 000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_B = 000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "SIM\_COLLISION\_CHECK = ALL" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "SRVAL\_A = 000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "SRVAL\_B = 000000000" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "WRITE\_MODE\_A = READ\_FIRST" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "WRITE\_MODE\_B = READ\_FIRST" for instance <ramgen\_l> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INITP\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_00 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_01 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_02 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_03 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_04 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_05 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_06 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_07 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_08 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_09 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_0F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_10 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_11 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_12 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_13 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_14 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_15 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_16 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_17 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_18 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_19 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_1A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_1B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_1C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_1D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_1E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_1F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_20 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_21 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_22 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_23 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_24 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_25 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_26 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_27 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_28 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_29 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_2A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_2B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_2C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_2D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_2E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_2F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_30 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_31 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_32 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_33 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_34 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_35 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_36 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_37 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_38 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_39 = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_3A = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_3B = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_3C = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_3D = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_3E = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_3F = 0000000000000000000000000000000000000000000000000000000000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_A = 000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "INIT\_B = 000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "SIM\_COLLISION\_CHECK = ALL" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "SRVAL\_A = 000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "SRVAL\_B = 000000000" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "WRITE\_MODE\_A = READ\_FIRST" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "WRITE\_MODE\_B = READ\_FIRST" for instance <ramgen\_u> in unit <rx\_client\_fifo\_8.2>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <wr\_rd\_addr\_gray\_sync>.

Set user-defined property "ASYNC\_REG = TRUE" for signal <rd\_store\_frame\_tog>.

Analyzing module <rx\_check> in library <work>.

ST\_DATA = 5'b00010

ST\_END = 5'b00100

ST\_IDLE = 5'b00000

ST\_LAST = 5'b00011

ST\_WAIT = 5'b00001

Module <rx\_check> is correct for synthesis.

Set user-defined property "KEEP = true" for signal <rx\_data> in unit <rx\_check>.

Set user-defined property "KEEP = true" for signal <rx\_sof> in unit <rx\_check>.

Set user-defined property "KEEP = true" for signal <rx\_eof> in unit <rx\_check>.

Set user-defined property "KEEP = true" for signal <rx\_src\_rdy> in unit <rx\_check>.

Set user-defined property "KEEP = true" for signal <IncrementByteCnt>.

Set user-defined property "KEEP = true" for signal <AddressOK>.

Set user-defined property "KEEP = true" for signal <ByteCntEq0>.

Set user-defined property "KEEP = true" for signal <ByteCntEq1>.

Set user-defined property "KEEP = true" for signal <ByteCntEq2>.

Set user-defined property "KEEP = true" for signal <ByteCntEq3>.

Set user-defined property "KEEP = true" for signal <ByteCntEq4>.

Set user-defined property "KEEP = true" for signal <ByteCntEq5>.

Set user-defined property "KEEP = true" for signal <ResetByteCnt>.

Set user-defined property "KEEP = true" for signal <ByteCntEq6>.

Set user-defined property "KEEP = true" for signal <ByteCntEq11>.

Set user-defined property "KEEP = true" for signal <ByteCntEq12>.

Set user-defined property "KEEP = true" for signal <ByteCntEq13>.

Set user-defined property "KEEP = true" for signal <ByteCntEq14>.

Set user-defined property "KEEP = true" for signal <ByteCntEq15>.

Set user-defined property "KEEP = true" for signal <ByteCntEq20>.

Set user-defined property "KEEP = true" for signal <ByteCntEq16>.

Set user-defined property "KEEP = true" for signal <ByteCntEq21>.

Set user-defined property "KEEP = true" for signal <ByteCntEq17>.

Set user-defined property "KEEP = true" for signal <ByteCntEq18>.

Set user-defined property "KEEP = true" for signal <ByteCntEq19>.

Set user-defined property "KEEP = true" for signal <cstate>.

Set user-defined property "KEEP = true" for signal <ByteCnt>.

Set user-defined property "KEEP = true" for signal <UnicastOK>.

Analyzing module <Div\_Ctrl> in library <work>.

TIM\_PRD = 32'b00000000101111101011110000100000

TIM\_PULSE = 32'b00000111011100110101100101000000

TIM\_RST\_FB = 32'b00000000000000011110100001001000

Module <Div\_Ctrl> is correct for synthesis.

Analyzing module <user\_spi\_flash\_ctrl> in library <work>.

st\_falsh\_cmd\_check\_WIP\_0 = 6'b011001

st\_falsh\_cmd\_check\_WIP\_1 = 6'b011010

st\_flash\_chk\_is\_on = 6'b001000

st\_flash\_chk\_is\_on\_1 = 6'b001001

st\_flash\_cmd\_ADDRH = 6'b010011

st\_flash\_cmd\_ADDRL = 6'b010101

st\_flash\_cmd\_ADDRM = 6'b010100

st\_flash\_cmd\_BE\_0 = 6'b001111

st\_flash\_cmd\_BE\_1 = 6'b010000

st\_flash\_cmd\_PP = 6'b010010

st\_flash\_cmd\_WREN = 6'b010001

st\_flash\_cmd\_data\_done = 6'b011000

st\_flash\_cmd\_data\_rd = 6'b010110

st\_flash\_cmd\_data\_wr = 6'b010111

st\_flash\_idle = 6'b000000

st\_flash\_init = 6'b000001

st\_flash\_rdid\_0 = 6'b001010

st\_flash\_rdid\_1 = 6'b001011

st\_flash\_rdid\_2 = 6'b001100

st\_flash\_rdid\_over = 6'b001101

st\_flash\_res\_0 = 6'b000010

st\_flash\_res\_1 = 6'b000011

st\_flash\_res\_2 = 6'b000100

st\_flash\_res\_3 = 6'b000101

st\_flash\_res\_4 = 6'b000110

st\_flash\_res\_5 = 6'b000111

st\_flash\_wait\_cmd = 6'b001110

st\_rx\_config\_data = 5'b01111

st\_rx\_config\_data\_0 = 5'b01010

st\_rx\_config\_data\_1 = 5'b01011

st\_rx\_config\_data\_2 = 5'b01100

st\_rx\_config\_data\_3 = 5'b01101

st\_rx\_config\_data\_4 = 5'b01110

st\_rx\_config\_data\_done = 5'b10000

st\_rx\_config\_head\_1 = 5'b00111

st\_rx\_config\_head\_2 = 5'b01000

st\_rx\_config\_head\_3 = 5'b01001

st\_rx\_config\_idle = 5'b00000

st\_rx\_config\_send\_msg = 5'b00010

st\_rx\_config\_wait\_1 = 5'b00011

st\_rx\_config\_wait\_2 = 5'b00100

st\_rx\_config\_wait\_3 = 5'b00101

st\_rx\_config\_wait\_be\_done = 5'b00001

st\_rx\_config\_wait\_cmd = 5'b00110

st\_rx\_config\_wait\_pp = 5'b10001

st\_rx\_config\_wait\_wip0 = 5'b11111

st\_wait\_sync\_chk0 = 3'b001

st\_wait\_sync\_chk1 = 3'b010

st\_wait\_sync\_chk2 = 3'b011

st\_wait\_sync\_chk3 = 3'b100

st\_wait\_sync\_idle = 3'b000

Enabling task <tx\_shift\_out>.

Enabling task <tx\_shift\_out>.

Enabling task <tx\_shift\_out>.

Enabling task <tx\_shift\_out>.

Enabling task <rx\_shift\_in>.

Enabling task <tx\_shift\_out>.

Enabling task <rx\_shift\_in>.

Enabling task <rx\_shift\_in>.

Enabling task <rx\_shift\_in>.

Enabling task <tx\_shift\_out>.

Enabling task <tx\_shift\_out>.

Enabling task <tx\_shift\_out>.

Enabling task <tx\_shift\_out>.

Enabling task <tx\_shift\_out>.

Enabling task <tx\_shift\_out>.

Enabling task <tx\_shift\_out>.

Enabling task <tx\_shift\_out>.

Enabling task <tx\_shift\_out>.

Enabling task <rx\_shift\_in>.

WARNING:Xst:2211 - "ipcore\_dir/dualPortRAM.v" line 1046: Instantiating black box module <dualPortRAM>.

Module <user\_spi\_flash\_ctrl> is correct for synthesis.

Set user-defined property "KEEP = true" for signal <tx\_ll\_sof> in unit <user\_spi\_flash\_ctrl>.

Set user-defined property "KEEP = true" for signal <tx\_ll\_eof> in unit <user\_spi\_flash\_ctrl>.

Set user-defined property "KEEP = true" for signal <tx\_ll\_src\_rdy> in unit <user\_spi\_flash\_ctrl>.

Set user-defined property "KEEP = true" for signal <tx\_ll\_data> in unit <user\_spi\_flash\_ctrl>.

Set user-defined property "KEEP = true" for signal <doutb>.

Set user-defined property "KEEP = true" for signal <ADDRH\_r>.

Set user-defined property "KEEP = true" for signal <spi\_nss\_r>.

Set user-defined property "KEEP = true" for signal <err\_pp>.

Set user-defined property "KEEP = true" for signal <tx\_sreg>.

Set user-defined property "KEEP = true" for signal <wait\_config\_sync\_flag>.

Set user-defined property "KEEP = true" for signal <is\_wip\_0>.

Set user-defined property "KEEP = true" for signal <mem\_cap>.

Set user-defined property "KEEP = true" for signal <pp\_cycle\_tim>.

Set user-defined property "KEEP = true" for signal <page\_len>.

Set user-defined property "KEEP = true" for signal <addra>.

Set user-defined property "KEEP = true" for signal <addrb>.

Set user-defined property "KEEP = true" for signal <rx\_sreg>.

Set user-defined property "KEEP = true" for signal <byteCnt>.

Set user-defined property "KEEP = true" for signal <status\_r>.

Set user-defined property "KEEP = true" for signal <hold\_sync\_flag\_high\_cnt>.

Set user-defined property "KEEP = true" for signal <wait\_data\_cnt>.

Set user-defined property "KEEP = true" for signal <ena>.

Set user-defined property "KEEP = true" for signal <enb>.

Set user-defined property "KEEP = true" for signal <tx\_bit\_cnt>.

Set user-defined property "KEEP = true" for signal <wea>.

Set user-defined property "KEEP = true" for signal <ADDRL\_r>.

Set user-defined property "KEEP = true" for signal <manu\_id>.

Set user-defined property "KEEP = true" for signal <wait\_be\_done\_cnt>.

Set user-defined property "KEEP = true" for signal <ADDRM\_r>.

Set user-defined property "KEEP = true" for signal <err\_rx\_data>.

Set user-defined property "KEEP = true" for signal <dina>.

Set user-defined property "KEEP = true" for signal <err\_be>.

Set user-defined property "KEEP = true" for signal <st\_flash\_op>.

Set user-defined property "KEEP = true" for signal <rx\_bit\_cnt>.

Set user-defined property "KEEP = true" for signal <st\_wait\_sync>.

Set user-defined property "KEEP = true" for signal <spi\_mosi\_r>.

Set user-defined property "KEEP = true" for signal <spi\_clk\_r>.

Set user-defined property "KEEP = true" for signal <page\_num>.

Set user-defined property "KEEP = true" for signal <res\_sign\_r>.

Set user-defined property "KEEP = true" for signal <mem\_type>.

Analyzing module <tx\_control> in library <work>.

TX\_DA1 = 16'b0000000000000001

TX\_DA2 = 16'b0000000000000010

TX\_DA3 = 16'b0000000000000100

TX\_DA4 = 16'b0000000000001000

TX\_DA5 = 16'b0000000000010000

TX\_DA6 = 16'b0000000000100000

TX\_DAT = 16'b0100000000000000

TX\_IDLE = 16'b0000000000000000

TX\_LEH = 16'b0001000000000000

TX\_LEL = 16'b0010000000000000

TX\_SA1 = 16'b0000000001000000

TX\_SA2 = 16'b0000000010000000

TX\_SA3 = 16'b0000000100000000

TX\_SA4 = 16'b0000001000000000

TX\_SA5 = 16'b0000010000000000

TX\_SA6 = 16'b0000100000000000

Module <tx\_control> is correct for synthesis.

Analyzing module <m25pxx\_spi\_flash\_ctrl> in library <work>.

ST\_IDLE = 8'b00000000

ST\_SPI\_CTRL\_0 = 8'b00000011

ST\_SPI\_INIT\_DIV = 8'b00000010

ST\_SPI\_INIT\_SS = 8'b00000001

ST\_SPI\_PP\_BRANCH = 8'b00111101

ST\_SPI\_PP\_CTRL\_GO\_ADDH = 8'b00110010

ST\_SPI\_PP\_CTRL\_GO\_ADDL = 8'b00111000

ST\_SPI\_PP\_CTRL\_GO\_ADDM = 8'b00110101

ST\_SPI\_PP\_CTRL\_GO\_CMD = 8'b00101111

ST\_SPI\_PP\_CTRL\_GO\_DATA = 8'b00111011

ST\_SPI\_PP\_SS\_CLEAR = 8'b00111110

ST\_SPI\_PP\_SS\_SET = 8'b00101110

ST\_SPI\_PP\_TX0\_ADDH = 8'b00110001

ST\_SPI\_PP\_TX0\_ADDL = 8'b00110111

ST\_SPI\_PP\_TX0\_ADDM = 8'b00110100

ST\_SPI\_PP\_TX0\_CMD = 8'b00101101

ST\_SPI\_PP\_TX0\_DATA = 8'b00111010

ST\_SPI\_PP\_WAIT\_ADDH = 8'b00110011

ST\_SPI\_PP\_WAIT\_ADDL = 8'b00111001

ST\_SPI\_PP\_WAIT\_ADDM = 8'b00110110

ST\_SPI\_PP\_WAIT\_CMD = 8'b00110000

ST\_SPI\_PP\_WAIT\_DATA = 8'b00111100

ST\_SPI\_PP\_WREN\_CTRL\_GO = 8'b00101010

ST\_SPI\_PP\_WREN\_SS\_CLEAR = 8'b00101100

ST\_SPI\_PP\_WREN\_SS\_SET = 8'b00101001

ST\_SPI\_PP\_WREN\_TX0 = 8'b00101000

ST\_SPI\_PP\_WREN\_WAIT = 8'b00101011

ST\_SPI\_RDID\_CTRL\_GO = 8'b00000110

ST\_SPI\_RDID\_RD\_DUMMY = 8'b00001000

ST\_SPI\_RDID\_SS\_CLEAR = 8'b00010010

ST\_SPI\_RDID\_SS\_SET\_RDID = 8'b00000101

ST\_SPI\_RDID\_TXCMD = 8'b00000100

ST\_SPI\_RDID\_TX\_DUMMY1 = 8'b00001001

ST\_SPI\_RDID\_TX\_DUMMY2 = 8'b00001100

ST\_SPI\_RDID\_TX\_DUMMY3 = 8'b00001111

ST\_SPI\_RDID\_WAIT0 = 8'b00000111

ST\_SPI\_RDID\_WAIT1 = 8'b00001010

ST\_SPI\_RDID\_WAIT2 = 8'b00001101

ST\_SPI\_RDID\_WAIT3 = 8'b00010000

ST\_SPI\_RDID\_manuID = 8'b00001011

ST\_SPI\_RDID\_memType = 8'b00001110

ST\_SPI\_RDID\_menCap = 8'b00010001

ST\_SPI\_RDSR\_BRANCH = 8'b00100110

ST\_SPI\_RDSR\_CTRL\_GO = 8'b00100000

ST\_SPI\_RDSR\_CTRL\_GO\_NOP = 8'b00100011

ST\_SPI\_RDSR\_READ = 8'b00100101

ST\_SPI\_RDSR\_SS\_CLEAR = 8'b00100111

ST\_SPI\_RDSR\_SS\_SET = 8'b00011111

ST\_SPI\_RDSR\_TX0 = 8'b00011110

ST\_SPI\_RDSR\_TX0\_NOP = 8'b00100010

ST\_SPI\_RDSR\_WAIT = 8'b00100001

ST\_SPI\_RDSR\_WAIT\_1 = 8'b00100100

ST\_SPI\_RD\_BRANCH = 8'b01001111

ST\_SPI\_RD\_CTRL\_GO\_ADDH = 8'b01000100

ST\_SPI\_RD\_CTRL\_GO\_ADDL = 8'b01001010

ST\_SPI\_RD\_CTRL\_GO\_ADDM = 8'b01000111

ST\_SPI\_RD\_CTRL\_GO\_CMD = 8'b01000001

ST\_SPI\_RD\_CTRL\_GO\_DATA = 8'b01001101

ST\_SPI\_RD\_SS\_CLEAR = 8'b01010000

ST\_SPI\_RD\_SS\_SET = 8'b01000000

ST\_SPI\_RD\_TX0\_ADDH = 8'b01000011

ST\_SPI\_RD\_TX0\_ADDL = 8'b01001001

ST\_SPI\_RD\_TX0\_ADDM = 8'b01000110

ST\_SPI\_RD\_TX0\_CMD = 8'b00111111

ST\_SPI\_RD\_TX0\_DATA = 8'b01001100

ST\_SPI\_RD\_WAIT\_ADDH = 8'b01000101

ST\_SPI\_RD\_WAIT\_ADDL = 8'b01001011

ST\_SPI\_RD\_WAIT\_ADDM = 8'b01001000

ST\_SPI\_RD\_WAIT\_CMD = 8'b01000010

ST\_SPI\_RD\_WAIT\_DATA = 8'b01001110

ST\_SPI\_SE\_CTRL\_GO = 8'b00011011

ST\_SPI\_SE\_SS\_CLEAR = 8'b00011101

ST\_SPI\_SE\_SS\_SET = 8'b00011010

ST\_SPI\_SE\_TX0 = 8'b00011001

ST\_SPI\_SE\_WAIT = 8'b00011100

ST\_SPI\_WAIT = 8'b00010011

ST\_SPI\_WREN\_CTRL\_GO = 8'b00010110

ST\_SPI\_WREN\_SS\_CLEAR = 8'b00011000

ST\_SPI\_WREN\_SS\_SET = 8'b00010101

ST\_SPI\_WREN\_TX0 = 8'b00010100

ST\_SPI\_WREN\_WAIT = 8'b00010111

Module <m25pxx\_spi\_flash\_ctrl> is correct for synthesis.

Set user-defined property "KEEP = TRUE" for signal <ss\_pad\_i>.

Set user-defined property "KEEP = TRUE" for signal <wb\_dat\_o>.

Set user-defined property "KEEP = TRUE" for signal <wb\_cyc\_i>.

Set user-defined property "KEEP = TRUE" for signal <wb\_ack\_o>.

Set user-defined property "KEEP = TRUE" for signal <wb\_we\_i>.

Set user-defined property "KEEP = TRUE" for signal <wb\_stb\_i>.

Set user-defined property "KEEP = TRUE" for signal <wb\_int\_o>.

Set user-defined property "KEEP = TRUE" for signal <wb\_adr\_i>.

Set user-defined property "KEEP = TRUE" for signal <wb\_dat\_i>.

Set user-defined property "KEEP = TRUE" for signal <wb\_sel\_i>.

Set user-defined property "KEEP = TRUE" for signal <memType>.

Set user-defined property "KEEP = TRUE" for signal <memCap>.

Set user-defined property "KEEP = TRUE" for signal <RW\_i>.

Set user-defined property "KEEP = TRUE" for signal <manuID>.

Analyzing module <spi\_top> in library <work>.

Tp = 32'sb00000000000000000000000000000001

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_top.v" line 145: Delay is ignored for synthesis.

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_top.v" line 147: Delay is ignored for synthesis.

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_top.v" line 154: Delay is ignored for synthesis.

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_top.v" line 156: Delay is ignored for synthesis.

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_top.v" line 166: Delay is ignored for synthesis.

WARNING:Xst:915 - Message (916) is reported only 5 times for each module.

Module <spi\_top> is correct for synthesis.

Analyzing module <spi\_clgen> in library <work>.

Tp = 32'sb00000000000000000000000000000001

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_clgen.v" line 74: Delay is ignored for synthesis.

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_clgen.v" line 78: Delay is ignored for synthesis.

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_clgen.v" line 80: Delay is ignored for synthesis.

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_clgen.v" line 88: Delay is ignored for synthesis.

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_clgen.v" line 90: Delay is ignored for synthesis.

WARNING:Xst:915 - Message (916) is reported only 5 times for each module.

Module <spi\_clgen> is correct for synthesis.

Analyzing module <spi\_shift> in library <work>.

Tp = 32'sb00000000000000000000000000000001

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_shift.v" line 95: Delay is ignored for synthesis.

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_shift.v" line 99: Delay is ignored for synthesis.

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_shift.v" line 101: Delay is ignored for synthesis.

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_shift.v" line 109: Delay is ignored for synthesis.

WARNING:Xst:916 - "\_rtl/spi/trunk/rtl/verilog/spi\_shift.v" line 111: Delay is ignored for synthesis.

WARNING:Xst:915 - Message (916) is reported only 5 times for each module.

Module <spi\_shift> is correct for synthesis.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

INFO:Xst:2679 - Register <ADDRL\_r> in unit <user\_spi\_flash\_ctrl> has a constant value of 00000000 during circuit operation. The register is replaced by logic.

INFO:Xst:2679 - Register <tx\_ll\_sof> in unit <user\_spi\_flash\_ctrl> has a constant value of 1 during circuit operation. The register is replaced by logic.

INFO:Xst:2679 - Register <tx\_ll\_eof> in unit <user\_spi\_flash\_ctrl> has a constant value of 1 during circuit operation. The register is replaced by logic.

INFO:Xst:2679 - Register <tx\_ll\_src\_rdy> in unit <user\_spi\_flash\_ctrl> has a constant value of 1 during circuit operation. The register is replaced by logic.

INFO:Xst:2679 - Register <tx\_ll\_data> in unit <user\_spi\_flash\_ctrl> has a constant value of 00000000 during circuit operation. The register is replaced by logic.

INFO:Xst:2679 - Register <pp\_cycle\_tim> in unit <user\_spi\_flash\_ctrl> has a constant value of 00000000000000000000000000000000 during circuit operation. The register is replaced by logic.

INFO:Xst:2679 - Register <flash\_addr24> in unit <m25pxx\_spi\_flash\_ctrl> has a constant value of 000101010010011000110111 during circuit operation. The register is replaced by logic.

Synthesizing Unit <Div\_Ctrl>.

Related source file is "\_rtl/Div\_Ctrl.v".

Found 4-bit register for signal <led>.

Found 32-bit up counter for signal <divr>.

Found 32-bit up counter for signal <divr2>.

Found 32-bit up counter for signal <TIM>.

Summary:

inferred 3 Counter(s).

inferred 4 D-type flip-flop(s).

Unit <Div\_Ctrl> synthesized.

Synthesizing Unit <tx\_control>.

Related source file is "\_rtl/tx\_control.v".

Found finite state machine <FSM\_0> for signal <cstate>.

-----------------------------------------------------------------------

| States | 16 |

| Transitions | 33 |

| Inputs | 3 |

| Outputs | 16 |

| Clock | tx\_ll\_clk (rising\_edge) |

| Reset | tx\_ll\_rst (positive) |

| Reset type | asynchronous |

| Reset State | 0000000000000000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found 8-bit register for signal <tx\_ll\_data\_out>.

Found 1-bit register for signal <tx\_ll\_sof\_n\_out>.

Found 1-bit register for signal <tx\_ll\_src\_rdy\_n\_out>.

Found 1-bit register for signal <tx\_ll\_eof\_n\_out>.

Found 16-bit comparator less for signal <cstate$cmp\_lt0000> created at line 206.

Found 16-bit subtractor for signal <cstate$sub0000> created at line 206.

Found 16-bit register for signal <data\_ctr>.

Found 16-bit adder for signal <data\_ctr$addsub0000> created at line 205.

Found 16-bit register for signal <data\_length>.

Summary:

inferred 1 Finite State Machine(s).

inferred 27 D-type flip-flop(s).

inferred 2 Adder/Subtractor(s).

inferred 1 Comparator(s).

Unit <tx\_control> synthesized.

Synthesizing Unit <rx\_check>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/rx\_check.v".

WARNING:Xst:647 - Input <rx\_ll\_sof\_in\_n> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:1580 - Signal <ByteCntEq6> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <ByteCntEq21> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <ByteCntEq20> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <ByteCntEq19> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <ByteCntEq18> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <ByteCntEq17> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <ByteCntEq16> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <ByteCntEq15> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <ByteCntEq13> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <ByteCntEq12> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <ByteCntEq11> with a "KEEP" property is assigned but never used. Related logic will not be removed.

Found finite state machine <FSM\_1> for signal <cstate>.

-----------------------------------------------------------------------

| States | 4 |

| Transitions | 7 |

| Inputs | 3 |

| Outputs | 4 |

| Clock | rx\_ll\_clock (rising\_edge) |

| Reset | rx\_ll\_reset (positive) |

| Reset type | asynchronous |

| Reset State | 00000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

WARNING:Xst:697 - FSM extraction is enabled. Signal <cstate> cannot be preserved.

Found 8-bit register for signal <rx\_data>.

Found 1-bit register for signal <rx\_sof>.

Found 1-bit register for signal <rx\_eof>.

Found 1-bit register for signal <rx\_src\_rdy>.

Found 8-bit comparator equal for signal <AddressOK$cmp\_eq0000> created at line 152.

Found 11-bit up counter for signal <ByteCnt>.

Found 1-bit register for signal <UnicastOK>.

Found 8-bit comparator equal for signal <UnicastOK$cmp\_eq0000> created at line 136.

Found 8-bit comparator equal for signal <UnicastOK$cmp\_eq0001> created at line 138.

Found 8-bit comparator equal for signal <UnicastOK$cmp\_eq0002> created at line 140.

Found 8-bit comparator equal for signal <UnicastOK$cmp\_eq0003> created at line 142.

Found 8-bit comparator equal for signal <UnicastOK$cmp\_eq0004> created at line 144.

Summary:

inferred 1 Finite State Machine(s).

inferred 1 Counter(s).

inferred 12 D-type flip-flop(s).

inferred 6 Comparator(s).

Unit <rx\_check> synthesized.

Synthesizing Unit <spi\_clgen>.

Related source file is "\_rtl/spi/trunk/rtl/verilog/spi\_clgen.v".

Found 1-bit register for signal <clk\_out>.

Found 1-bit register for signal <pos\_edge>.

Found 1-bit register for signal <neg\_edge>.

Found 8-bit down counter for signal <cnt>.

Summary:

inferred 1 Counter(s).

inferred 3 D-type flip-flop(s).

Unit <spi\_clgen> synthesized.

Synthesizing Unit <spi\_shift>.

Related source file is "\_rtl/spi/trunk/rtl/verilog/spi\_shift.v".

WARNING:Xst:647 - Input <latch<3:1>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:647 - Input <p\_in<31:8>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:647 - Input <byte\_sel<3:1>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:646 - Signal <tx\_bit\_pos<3>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rx\_bit\_pos<3>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Found 1-bit register for signal <s\_out>.

Found 1-bit register for signal <tip>.

Found 4-bit register for signal <cnt>.

Found 8-bit register for signal <data>.

Found 4-bit subtractor for signal <rx\_bit\_pos$addsub0000> created at line 83.

Found 4-bit adder for signal <rx\_bit\_pos$addsub0001> created at line 83.

Found 4-bit subtractor for signal <tx\_bit\_pos$addsub0000> created at line 82.

Found 4-bit subtractor for signal <tx\_bit\_pos$sub0000> created at line 82.

Summary:

inferred 14 D-type flip-flop(s).

inferred 4 Adder/Subtractor(s).

inferred 2 Multiplexer(s).

Unit <spi\_shift> synthesized.

Synthesizing Unit <user\_spi\_flash\_ctrl>.

Related source file is "\_rtl/user\_spi\_flash\_ctrl.v".

WARNING:Xst:1580 - Signal <status\_r> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:653 - Signal <spi\_miso\_r> is used but never assigned. This sourceless signal will be automatically connected to value 0.

WARNING:Xst:1580 - Signal <spi\_clk\_r> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <res\_sign\_r> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <pp\_cycle\_tim> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <page\_num> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <mem\_type> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <mem\_cap> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <manu\_id> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <err\_rx\_data> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <err\_pp> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <err\_be> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1780 - Signal <enb> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <ena> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

Found finite state machine <FSM\_2> for signal <st\_wait\_sync>.

-----------------------------------------------------------------------

| States | 5 |

| Transitions | 15 |

| Inputs | 5 |

| Outputs | 3 |

| Clock | clk125m (rising\_edge) |

| Reset | rst\_n (negative) |

| Reset type | asynchronous |

| Reset State | 000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

WARNING:Xst:697 - FSM extraction is enabled. Signal <st\_wait\_sync> cannot be preserved.

Found finite state machine <FSM\_3> for signal <st\_rx\_config>.

-----------------------------------------------------------------------

| States | 19 |

| Transitions | 37 |

| Inputs | 12 |

| Outputs | 14 |

| Clock | clk125m (rising\_edge) |

| Reset | rst\_n (negative) |

| Reset type | asynchronous |

| Reset State | 00000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found finite state machine <FSM\_4> for signal <st\_flash\_op>.

-----------------------------------------------------------------------

| States | 27 |

| Transitions | 56 |

| Inputs | 10 |

| Outputs | 32 |

| Clock | clk\_i (rising\_edge) |

| Reset | rst\_n (negative) |

| Reset type | asynchronous |

| Reset State | 000000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

WARNING:Xst:697 - FSM extraction is enabled. Signal <st\_flash\_op> cannot be preserved.

Found 1-bit register for signal <send\_confirm\_msg\_flag>.

Found 10-bit register for signal <addra>.

Found 10-bit adder for signal <addra$addsub0000> created at line 380.

Found 10-bit up counter for signal <addrb>.

Found 8-bit register for signal <ADDRH\_r>.

Found 8-bit register for signal <ADDRM\_r>.

Found 11-bit register for signal <byteCnt>.

Found 11-bit adder for signal <byteCnt$addsub0000> created at line 383.

Found 8-bit register for signal <dina>.

Found 1-bit register for signal <err\_be>.

Found 1-bit register for signal <err\_pp>.

Found 1-bit register for signal <err\_rx\_data>.

Found 3-bit register for signal <hold\_sync\_flag\_high\_cnt>.

Found 3-bit adder for signal <hold\_sync\_flag\_high\_cnt$addsub0000> created at line 144.

Found 1-bit register for signal <is\_wip\_0>.

Found 8-bit register for signal <manu\_id>.

Found 8-bit register for signal <mem\_cap>.

Found 8-bit register for signal <mem\_type>.

Found 16-bit register for signal <page\_len>.

Found 16-bit register for signal <page\_num>.

Found 8-bit register for signal <res\_sign\_r>.

Found 5-bit register for signal <rx\_bit\_cnt>.

Found 5-bit adder for signal <rx\_bit\_cnt$addsub0000>.

Found 8-bit register for signal <rx\_sreg>.

Found 1-bit register for signal <spi\_clk\_r>.

Found 1-bit register for signal <spi\_mosi\_r>.

Found 1-bit register for signal <spi\_nss\_r>.

Found 5-bit comparator lessequal for signal <st\_flash\_op$cmp\_le0000> created at line 509.

Found 5-bit comparator lessequal for signal <st\_flash\_op$cmp\_le0001> created at line 533.

Found 5-bit comparator lessequal for signal <st\_flash\_op$cmp\_le0002> created at line 581.

Found 16-bit comparator less for signal <st\_flash\_op$cmp\_lt0000> created at line 798.

Found 1-bit register for signal <start\_pp>.

Found 8-bit register for signal <status\_r>.

Found 5-bit register for signal <tx\_bit\_cnt>.

Found 5-bit adder for signal <tx\_bit\_cnt$share0000> created at line 505.

Found 8-bit register for signal <tx\_sreg>.

Found 32-bit register for signal <wait\_be\_done\_cnt>.

Found 32-bit adder for signal <wait\_be\_done\_cnt$addsub0000> created at line 288.

Found 1-bit register for signal <wait\_config\_sync\_flag>.

Found 32-bit register for signal <wait\_data\_cnt>.

Found 32-bit adder for signal <wait\_data\_cnt$addsub0000> created at line 319.

Found 5-bit register for signal <wait\_pp\_cnt>.

Found 5-bit adder for signal <wait\_pp\_cnt$addsub0000> created at line 393.

Found 32-bit register for signal <wait\_wip\_chk\_cnt>.

Found 32-bit adder for signal <wait\_wip\_chk\_cnt$addsub0000> created at line 408.

Found 1-bit register for signal <wea>.

Summary:

inferred 3 Finite State Machine(s).

inferred 1 Counter(s).

inferred 258 D-type flip-flop(s).

inferred 9 Adder/Subtractor(s).

inferred 4 Comparator(s).

Unit <user\_spi\_flash\_ctrl> synthesized.

Synthesizing Unit <ethmac\_v1\_8>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8.v".

WARNING:Xst:646 - Signal <client\_rx\_data\_1\_i<15:8>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <client\_rx\_data\_0\_i<15:8>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Unit <ethmac\_v1\_8> synthesized.

Synthesizing Unit <ROCKETIO\_WRAPPER\_GTP\_TILE>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/physical/rocketio\_wrapper\_gtp\_tile.v".

WARNING:Xst:646 - Signal <tied\_to\_vcc\_vec\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rxrundisp1\_float\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rxrundisp0\_float\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rxnotintable1\_float\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rxnotintable0\_float\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rxdisperr1\_float\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rxdisperr0\_float\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rxdata1\_i<15:8>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rxdata0\_i<15:8>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rxcharisk1\_float\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rxcharisk0\_float\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rxchariscomma1\_float\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rxchariscomma0\_float\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Unit <ROCKETIO\_WRAPPER\_GTP\_TILE> synthesized.

Synthesizing Unit <tx\_client\_fifo\_8\_1>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/tx\_client\_fifo\_8.v".

INFO:Xst:2117 - HDL ADVISOR - Mux Selector <wr\_state> of Case statement line 323 was re-encoded using one-hot encoding. The case statement will be optimized (default statement optimization), but this optimization may lead to design initialization problems. To ensure the design works safely, you can:

- add an 'INIT' attribute on signal <wr\_state> (optimization is then done without any risk)

- use the attribute 'signal\_encoding user' to avoid onehot optimization

- use the attribute 'safe\_implementation yes' to force XST to perform a safe (but less efficient) optimization

Found finite state machine <FSM\_5> for signal <wr\_state>.

-----------------------------------------------------------------------

| States | 4 |

| Transitions | 11 |

| Inputs | 5 |

| Outputs | 6 |

| Clock | wr\_clk (rising\_edge) |

| Reset | wr\_sreset (positive) |

| Reset type | synchronous |

| Reset State | 00 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found finite state machine <FSM\_6> for signal <rd\_state>.

-----------------------------------------------------------------------

| States | 9 |

| Transitions | 21 |

| Inputs | 5 |

| Outputs | 9 |

| Clock | rd\_clk (rising\_edge) |

| Reset | rd\_sreset (positive) |

| Reset type | synchronous |

| Reset State | 0000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found 8-bit register for signal <tx\_data>.

Found 1-bit register for signal <tx\_data\_valid>.

Found 4-bit register for signal <wr\_fifo\_status>.

Found 1-bit register for signal <frame\_in\_fifo>.

Found 1-bit register for signal <frame\_in\_fifo\_sync>.

Found 4-bit up counter for signal <rd\_16\_count>.

Found 12-bit register for signal <rd\_addr>.

Found 12-bit adder for signal <rd\_addr$addsub0000> created at line 880.

Found 12-bit register for signal <rd\_addr\_txfer>.

Found 1-bit register for signal <rd\_bram\_u>.

Found 1-bit register for signal <rd\_bram\_u\_reg>.

Found 1-bit register for signal <rd\_col\_window\_expire>.

Found 2-bit register for signal <rd\_col\_window\_pipe>.

Found 8-bit register for signal <rd\_data\_pipe>.

Found 8-bit register for signal <rd\_data\_pipe\_l>.

Found 8-bit register for signal <rd\_data\_pipe\_u>.

Found 12-bit register for signal <rd\_dec\_addr>.

Found 12-bit subtractor for signal <rd\_dec\_addr$sub0000> created at line 946.

Found 1-bit register for signal <rd\_drop\_frame>.

Found 1-bit register for signal <rd\_enable\_delay>.

Found 1-bit register for signal <rd\_enable\_delay2>.

Found 1-bit register for signal <rd\_eof>.

Found 1-bit register for signal <rd\_eof\_pipe>.

Found 1-bit register for signal <rd\_eof\_reg>.

Found 1-bit register for signal <rd\_retran\_frame\_tog>.

Found 1-bit register for signal <rd\_retransmit>.

Found 10-bit up counter for signal <rd\_slot\_timer>.

Found 12-bit register for signal <rd\_start\_addr>.

Found 12-bit subtractor for signal <rd\_start\_addr$sub0000> created at line 889.

Found 1-bit register for signal <rd\_tran\_frame\_tog>.

Found 1-bit register for signal <rd\_txfer\_tog>.

Found 1-bit register for signal <wr\_accept\_bram>.

Found 2-bit register for signal <wr\_accept\_pipe>.

Found 12-bit up counter for signal <wr\_addr>.

Found 12-bit register for signal <wr\_addr\_diff>.

Found 12-bit subtractor for signal <wr\_addr\_diff$sub0000> created at line 1142.

Found 1-bit register for signal <wr\_col\_window\_expire>.

Found 2-bit register for signal <wr\_col\_window\_pipe>.

Found 8-bit register for signal <wr\_data\_bram>.

Found 16-bit register for signal <wr\_data\_pipe>.

Found 1-bit register for signal <wr\_eof\_bram<0>>.

Found 2-bit register for signal <wr\_eof\_pipe>.

Found 1-bit register for signal <wr\_eof\_state\_reg>.

Found 1-bit register for signal <wr\_fifo\_full>.

Found 1-bit register for signal <wr\_frame\_in\_fifo>.

Found 9-bit updown counter for signal <wr\_frames>.

Found 9-bit adder for signal <wr\_frames$add0000> created at line 775.

Found 1-bit register for signal <wr\_ovflow\_dst\_rdy>.

Found 12-bit register for signal <wr\_rd\_addr>.

Found 1-bit register for signal <wr\_retran\_frame\_delay>.

Found 1-bit register for signal <wr\_retran\_frame\_sync>.

Found 1-bit register for signal <wr\_retran\_frame\_tog>.

Found 1-bit register for signal <wr\_retransmit\_frame>.

Found 1-bit xor2 for signal <wr\_retransmit\_frame$xor0000> created at line 758.

Found 2-bit register for signal <wr\_sof\_pipe>.

Found 12-bit register for signal <wr\_start\_addr>.

Found 12-bit adder for signal <wr\_start\_addr$add0000> created at line 835.

Found 1-bit register for signal <wr\_tran\_frame\_delay>.

Found 1-bit register for signal <wr\_tran\_frame\_sync>.

Found 1-bit register for signal <wr\_tran\_frame\_tog>.

Found 1-bit register for signal <wr\_transmit\_frame>.

Found 1-bit xor2 for signal <wr\_transmit\_frame$xor0000> created at line 701.

Found 1-bit xor2 for signal <wr\_txfer\_en>.

Found 1-bit register for signal <wr\_txfer\_tog>.

Found 1-bit register for signal <wr\_txfer\_tog\_delay>.

Found 1-bit register for signal <wr\_txfer\_tog\_sync>.

Summary:

inferred 2 Finite State Machine(s).

inferred 4 Counter(s).

inferred 188 D-type flip-flop(s).

inferred 6 Adder/Subtractor(s).

Unit <tx\_client\_fifo\_8\_1> synthesized.

Synthesizing Unit <rx\_client\_fifo\_8\_1>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/rx\_client\_fifo\_8.v".

WARNING:Xst:646 - Signal <rd\_valid\_pipe<2>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

INFO:Xst:2117 - HDL ADVISOR - Mux Selector <rd\_state> of Case statement line 308 was re-encoded using one-hot encoding. The case statement will be optimized (default statement optimization), but this optimization may lead to design initialization problems. To ensure the design works safely, you can:

- add an 'INIT' attribute on signal <rd\_state> (optimization is then done without any risk)

- use the attribute 'signal\_encoding user' to avoid onehot optimization

- use the attribute 'safe\_implementation yes' to force XST to perform a safe (but less efficient) optimization

Found finite state machine <FSM\_7> for signal <rd\_state>.

-----------------------------------------------------------------------

| States | 8 |

| Transitions | 15 |

| Inputs | 5 |

| Outputs | 17 |

| Clock | rd\_clk (rising\_edge) |

| Reset | rd\_sreset (positive) |

| Reset type | synchronous |

| Reset State | 000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found finite state machine <FSM\_8> for signal <wr\_state>.

-----------------------------------------------------------------------

| States | 6 |

| Transitions | 15 |

| Inputs | 5 |

| Outputs | 5 |

| Clock | wr\_clk (rising\_edge) |

| Reset | wr\_sreset (positive) |

| Reset type | synchronous |

| Reset State | 000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found 8-bit register for signal <rd\_data\_out>.

Found 1-bit register for signal <rd\_src\_rdy\_n>.

Found 1-bit register for signal <rd\_sof\_n>.

Found 11-bit xor2 for signal <bin\_to\_gray/1/bin\_to\_gray<10:0>>.

Found 1-bit register for signal <frame\_in\_fifo>.

Found 1-bit xor2 for signal <gray\_to\_bin/1/gray\_to\_bin<0>>.

Found 12-bit updown accumulator for signal <rd\_addr>.

Found 12-bit register for signal <rd\_addr\_gray>.

Found 1-bit register for signal <rd\_bram\_u>.

Found 1-bit register for signal <rd\_bram\_u\_reg>.

Found 8-bit register for signal <rd\_data\_pipe>.

Found 8-bit register for signal <rd\_data\_pipe\_l>.

Found 8-bit register for signal <rd\_data\_pipe\_u>.

Found 1-bit register for signal <rd\_eof>.

Found 1-bit register for signal <rd\_eof\_n\_int>.

Found 9-bit updown counter for signal <rd\_frames>.

Found 1-bit register for signal <rd\_store\_frame>.

Found 1-bit xor2 for signal <rd\_store\_frame$xor0000> created at line 511.

Found 1-bit register for signal <rd\_store\_frame\_delay>.

Found 1-bit register for signal <rd\_store\_frame\_sync>.

Found 1-bit register for signal <rd\_store\_frame\_tog>.

Found 3-bit register for signal <rd\_valid\_pipe>.

Found 12-bit up counter for signal <wr\_addr>.

Found 12-bit register for signal <wr\_addr\_diff>.

Found 12-bit subtractor for signal <wr\_addr\_diff$sub0000> created at line 803.

Found 2-bit register for signal <wr\_bf\_pipe>.

Found 8-bit register for signal <wr\_data\_bram>.

Found 16-bit register for signal <wr\_data\_pipe>.

Found 2-bit register for signal <wr\_dv\_pipe>.

Found 1-bit register for signal <wr\_eof\_bram<0>>.

Found 1-bit register for signal <wr\_fifo\_full>.

Found 4-bit register for signal <wr\_fifo\_status>.

Found 2-bit register for signal <wr\_gf\_pipe>.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0000> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0001> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0002> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0003> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0004> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0005> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0006> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0007> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0008> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0009> created at line 274.

Found 12-bit register for signal <wr\_rd\_addr\_gray>.

Found 12-bit register for signal <wr\_rd\_addr\_gray\_sync>.

Found 12-bit register for signal <wr\_start\_addr>.

Found 1-bit register for signal <wr\_store\_frame\_tog>.

Summary:

inferred 2 Finite State Machine(s).

inferred 2 Counter(s).

inferred 1 Accumulator(s).

inferred 143 D-type flip-flop(s).

inferred 1 Adder/Subtractor(s).

Unit <rx\_client\_fifo\_8\_1> synthesized.

Synthesizing Unit <tx\_client\_fifo\_8\_2>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/tx\_client\_fifo\_8.v".

INFO:Xst:2117 - HDL ADVISOR - Mux Selector <wr\_state> of Case statement line 323 was re-encoded using one-hot encoding. The case statement will be optimized (default statement optimization), but this optimization may lead to design initialization problems. To ensure the design works safely, you can:

- add an 'INIT' attribute on signal <wr\_state> (optimization is then done without any risk)

- use the attribute 'signal\_encoding user' to avoid onehot optimization

- use the attribute 'safe\_implementation yes' to force XST to perform a safe (but less efficient) optimization

Found finite state machine <FSM\_9> for signal <wr\_state>.

-----------------------------------------------------------------------

| States | 4 |

| Transitions | 11 |

| Inputs | 5 |

| Outputs | 6 |

| Clock | wr\_clk (rising\_edge) |

| Reset | wr\_sreset (positive) |

| Reset type | synchronous |

| Reset State | 00 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found finite state machine <FSM\_10> for signal <rd\_state>.

-----------------------------------------------------------------------

| States | 9 |

| Transitions | 21 |

| Inputs | 5 |

| Outputs | 9 |

| Clock | rd\_clk (rising\_edge) |

| Reset | rd\_sreset (positive) |

| Reset type | synchronous |

| Reset State | 0000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found 8-bit register for signal <tx\_data>.

Found 1-bit register for signal <tx\_data\_valid>.

Found 4-bit register for signal <wr\_fifo\_status>.

Found 1-bit register for signal <frame\_in\_fifo>.

Found 1-bit register for signal <frame\_in\_fifo\_sync>.

Found 4-bit up counter for signal <rd\_16\_count>.

Found 12-bit register for signal <rd\_addr>.

Found 12-bit adder for signal <rd\_addr$addsub0000> created at line 880.

Found 12-bit register for signal <rd\_addr\_txfer>.

Found 1-bit register for signal <rd\_bram\_u>.

Found 1-bit register for signal <rd\_bram\_u\_reg>.

Found 1-bit register for signal <rd\_col\_window\_expire>.

Found 2-bit register for signal <rd\_col\_window\_pipe>.

Found 8-bit register for signal <rd\_data\_pipe>.

Found 8-bit register for signal <rd\_data\_pipe\_l>.

Found 8-bit register for signal <rd\_data\_pipe\_u>.

Found 12-bit register for signal <rd\_dec\_addr>.

Found 12-bit subtractor for signal <rd\_dec\_addr$sub0000> created at line 946.

Found 1-bit register for signal <rd\_drop\_frame>.

Found 1-bit register for signal <rd\_enable\_delay>.

Found 1-bit register for signal <rd\_enable\_delay2>.

Found 1-bit register for signal <rd\_eof>.

Found 1-bit register for signal <rd\_eof\_pipe>.

Found 1-bit register for signal <rd\_eof\_reg>.

Found 1-bit register for signal <rd\_retran\_frame\_tog>.

Found 1-bit register for signal <rd\_retransmit>.

Found 10-bit up counter for signal <rd\_slot\_timer>.

Found 12-bit register for signal <rd\_start\_addr>.

Found 12-bit subtractor for signal <rd\_start\_addr$sub0000> created at line 889.

Found 1-bit register for signal <rd\_tran\_frame\_tog>.

Found 1-bit register for signal <rd\_txfer\_tog>.

Found 1-bit register for signal <wr\_accept\_bram>.

Found 2-bit register for signal <wr\_accept\_pipe>.

Found 12-bit up counter for signal <wr\_addr>.

Found 12-bit register for signal <wr\_addr\_diff>.

Found 12-bit subtractor for signal <wr\_addr\_diff$sub0000> created at line 1142.

Found 1-bit register for signal <wr\_col\_window\_expire>.

Found 2-bit register for signal <wr\_col\_window\_pipe>.

Found 8-bit register for signal <wr\_data\_bram>.

Found 16-bit register for signal <wr\_data\_pipe>.

Found 1-bit register for signal <wr\_eof\_bram<0>>.

Found 2-bit register for signal <wr\_eof\_pipe>.

Found 1-bit register for signal <wr\_eof\_state\_reg>.

Found 1-bit register for signal <wr\_fifo\_full>.

Found 1-bit register for signal <wr\_frame\_in\_fifo>.

Found 9-bit updown counter for signal <wr\_frames>.

Found 9-bit adder for signal <wr\_frames$add0000> created at line 775.

Found 1-bit register for signal <wr\_ovflow\_dst\_rdy>.

Found 12-bit register for signal <wr\_rd\_addr>.

Found 1-bit register for signal <wr\_retran\_frame\_delay>.

Found 1-bit register for signal <wr\_retran\_frame\_sync>.

Found 1-bit register for signal <wr\_retran\_frame\_tog>.

Found 1-bit register for signal <wr\_retransmit\_frame>.

Found 1-bit xor2 for signal <wr\_retransmit\_frame$xor0000> created at line 758.

Found 2-bit register for signal <wr\_sof\_pipe>.

Found 12-bit register for signal <wr\_start\_addr>.

Found 12-bit adder for signal <wr\_start\_addr$add0000> created at line 835.

Found 1-bit register for signal <wr\_tran\_frame\_delay>.

Found 1-bit register for signal <wr\_tran\_frame\_sync>.

Found 1-bit register for signal <wr\_tran\_frame\_tog>.

Found 1-bit register for signal <wr\_transmit\_frame>.

Found 1-bit xor2 for signal <wr\_transmit\_frame$xor0000> created at line 701.

Found 1-bit xor2 for signal <wr\_txfer\_en>.

Found 1-bit register for signal <wr\_txfer\_tog>.

Found 1-bit register for signal <wr\_txfer\_tog\_delay>.

Found 1-bit register for signal <wr\_txfer\_tog\_sync>.

Summary:

inferred 2 Finite State Machine(s).

inferred 4 Counter(s).

inferred 188 D-type flip-flop(s).

inferred 6 Adder/Subtractor(s).

Unit <tx\_client\_fifo\_8\_2> synthesized.

Synthesizing Unit <rx\_client\_fifo\_8\_2>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/rx\_client\_fifo\_8.v".

WARNING:Xst:646 - Signal <rd\_valid\_pipe<2>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

INFO:Xst:2117 - HDL ADVISOR - Mux Selector <rd\_state> of Case statement line 308 was re-encoded using one-hot encoding. The case statement will be optimized (default statement optimization), but this optimization may lead to design initialization problems. To ensure the design works safely, you can:

- add an 'INIT' attribute on signal <rd\_state> (optimization is then done without any risk)

- use the attribute 'signal\_encoding user' to avoid onehot optimization

- use the attribute 'safe\_implementation yes' to force XST to perform a safe (but less efficient) optimization

Found finite state machine <FSM\_11> for signal <rd\_state>.

-----------------------------------------------------------------------

| States | 8 |

| Transitions | 15 |

| Inputs | 5 |

| Outputs | 17 |

| Clock | rd\_clk (rising\_edge) |

| Reset | rd\_sreset (positive) |

| Reset type | synchronous |

| Reset State | 000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found finite state machine <FSM\_12> for signal <wr\_state>.

-----------------------------------------------------------------------

| States | 6 |

| Transitions | 15 |

| Inputs | 5 |

| Outputs | 5 |

| Clock | wr\_clk (rising\_edge) |

| Reset | wr\_sreset (positive) |

| Reset type | synchronous |

| Reset State | 000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found 8-bit register for signal <rd\_data\_out>.

Found 1-bit register for signal <rd\_src\_rdy\_n>.

Found 1-bit register for signal <rd\_sof\_n>.

Found 11-bit xor2 for signal <bin\_to\_gray/1/bin\_to\_gray<10:0>>.

Found 1-bit register for signal <frame\_in\_fifo>.

Found 1-bit xor2 for signal <gray\_to\_bin/1/gray\_to\_bin<0>>.

Found 12-bit updown accumulator for signal <rd\_addr>.

Found 12-bit register for signal <rd\_addr\_gray>.

Found 1-bit register for signal <rd\_bram\_u>.

Found 1-bit register for signal <rd\_bram\_u\_reg>.

Found 8-bit register for signal <rd\_data\_pipe>.

Found 8-bit register for signal <rd\_data\_pipe\_l>.

Found 8-bit register for signal <rd\_data\_pipe\_u>.

Found 1-bit register for signal <rd\_eof>.

Found 1-bit register for signal <rd\_eof\_n\_int>.

Found 9-bit updown counter for signal <rd\_frames>.

Found 1-bit register for signal <rd\_store\_frame>.

Found 1-bit xor2 for signal <rd\_store\_frame$xor0000> created at line 511.

Found 1-bit register for signal <rd\_store\_frame\_delay>.

Found 1-bit register for signal <rd\_store\_frame\_sync>.

Found 1-bit register for signal <rd\_store\_frame\_tog>.

Found 3-bit register for signal <rd\_valid\_pipe>.

Found 12-bit up counter for signal <wr\_addr>.

Found 12-bit register for signal <wr\_addr\_diff>.

Found 12-bit subtractor for signal <wr\_addr\_diff$sub0000> created at line 803.

Found 2-bit register for signal <wr\_bf\_pipe>.

Found 8-bit register for signal <wr\_data\_bram>.

Found 16-bit register for signal <wr\_data\_pipe>.

Found 2-bit register for signal <wr\_dv\_pipe>.

Found 1-bit register for signal <wr\_eof\_bram<0>>.

Found 1-bit register for signal <wr\_fifo\_full>.

Found 4-bit register for signal <wr\_fifo\_status>.

Found 2-bit register for signal <wr\_gf\_pipe>.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0000> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0001> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0002> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0003> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0004> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0005> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0006> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0007> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0008> created at line 274.

Found 1-bit xor2 for signal <wr\_rd\_addr$xor0009> created at line 274.

Found 12-bit register for signal <wr\_rd\_addr\_gray>.

Found 12-bit register for signal <wr\_rd\_addr\_gray\_sync>.

Found 12-bit register for signal <wr\_start\_addr>.

Found 1-bit register for signal <wr\_store\_frame\_tog>.

Summary:

inferred 2 Finite State Machine(s).

inferred 2 Counter(s).

inferred 1 Accumulator(s).

inferred 143 D-type flip-flop(s).

inferred 1 Adder/Subtractor(s).

Unit <rx\_client\_fifo\_8\_2> synthesized.

Synthesizing Unit <spi\_top>.

Related source file is "\_rtl/spi/trunk/rtl/verilog/spi\_top.v".

WARNING:Xst:647 - Input <wb\_adr\_i<4:3>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Found 1-bit register for signal <wb\_int\_o>.

Found 32-bit register for signal <wb\_dat\_o>.

Found 1-bit register for signal <wb\_ack\_o>.

Found 14-bit register for signal <ctrl>.

Found 8-bit register for signal <divider>.

Found 8-bit register for signal <ss>.

Found 32-bit 7-to-1 multiplexer for signal <wb\_dat>.

Summary:

inferred 64 D-type flip-flop(s).

inferred 32 Multiplexer(s).

Unit <spi\_top> synthesized.

Synthesizing Unit <m25pxx\_spi\_flash\_ctrl>.

Related source file is "\_rtl/m25pxx\_spi\_flash\_ctrl.v".

WARNING:Xst:1580 - Signal <wb\_dat\_o<31:8>> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <ss\_pad\_i<7:1>> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <memType> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <memCap> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:1580 - Signal <manuID> with a "KEEP" property is assigned but never used. Related logic will not be removed.

WARNING:Xst:646 - Signal <dout\_read> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Found finite state machine <FSM\_13> for signal <cstate>.

-----------------------------------------------------------------------

| States | 81 |

| Transitions | 192 |

| Inputs | 9 |

| Outputs | 81 |

| Clock | clk\_i (rising\_edge) |

| Reset | rst\_n (negative) |

| Reset type | asynchronous |

| Reset State | 00000000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Found 16-bit comparator greatequal for signal <cstate$cmp\_ge0000> created at line 225.

Found 9-bit comparator greater for signal <cstate$cmp\_gt0000> created at line 440.

Found 9-bit comparator greater for signal <cstate$cmp\_gt0001> created at line 497.

Found 8-bit register for signal <din\_to\_pp>.

Found 8-bit register for signal <manuID>.

Found 8-bit register for signal <memCap>.

Found 8-bit register for signal <memType>.

Found 16-bit register for signal <por\_rst\_delay\_cnt>.

Found 16-bit adder for signal <por\_rst\_delay\_cnt$addsub0000> created at line 543.

Found 9-bit up counter for signal <pp\_bytes\_cnt>.

Found 32-bit up counter for signal <rdsr\_cnt>.

Found 9-bit up counter for signal <read\_bytes\_cnt>.

Found 3-bit register for signal <RW\_i>.

Found 16-bit comparator greatequal for signal <RW\_i$cmp\_ge0000> created at line 544.

Found 16-bit comparator lessequal for signal <RW\_i$cmp\_le0000> created at line 544.

Found 5-bit register for signal <wb\_adr\_i>.

Found 32-bit register for signal <wb\_dat\_i>.

Found 4-bit register for signal <wb\_sel\_i>.

Found 1-bit register for signal <WIP\_r>.

Summary:

inferred 1 Finite State Machine(s).

inferred 3 Counter(s).

inferred 93 D-type flip-flop(s).

inferred 1 Adder/Subtractor(s).

inferred 5 Comparator(s).

Unit <m25pxx\_spi\_flash\_ctrl> synthesized.

Synthesizing Unit <eth\_fifo\_8\_1>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/eth\_fifo\_8.v".

Unit <eth\_fifo\_8\_1> synthesized.

Synthesizing Unit <eth\_fifo\_8\_2>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/client/fifo/eth\_fifo\_8.v".

Unit <eth\_fifo\_8\_2> synthesized.

Synthesizing Unit <ROCKETIO\_WRAPPER\_GTP>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/physical/rocketio\_wrapper\_gtp.v".

WARNING:Xst:646 - Signal <tied\_to\_vcc\_vec\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <tied\_to\_vcc\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <tied\_to\_ground\_vec\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <tied\_to\_ground\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Unit <ROCKETIO\_WRAPPER\_GTP> synthesized.

Synthesizing Unit <GTP\_dual\_1000X>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/physical/gtp\_dual\_1000X.v".

WARNING:Xst:647 - Input <RXUSRCLK2\_0> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:647 - Input <RXUSRCLK2\_1> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:647 - Input <PMARESET> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:647 - Input <DCM\_LOCKED> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:646 - Signal <TXBUFSTATUS\_float1> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <TXBUFSTATUS\_float0> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <RXBUFSTATUS\_float1> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <RXBUFSTATUS\_float0> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Unit <GTP\_dual\_1000X> synthesized.

Synthesizing Unit <ethmac\_v1\_8\_block>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_block.v".

WARNING:Xst:1780 - Signal <tx\_reset\_sm\_1\_r> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <tx\_reset\_sm\_0\_r> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <tx\_pcs\_reset\_1\_r> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <tx\_pcs\_reset\_0\_r> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <tx\_client\_clk\_out\_1\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <tx\_client\_clk\_out\_0\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <rxlossofsync\_1\_i> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <rxlossofsync\_0\_i> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:653 - Signal <rxbufstatus\_1\_i<0>> is used but never assigned. This sourceless signal will be automatically connected to value 0.

WARNING:Xst:653 - Signal <rxbufstatus\_0\_i<0>> is used but never assigned. This sourceless signal will be automatically connected to value 0.

WARNING:Xst:1780 - Signal <rx\_reset\_sm\_1\_r> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <rx\_reset\_sm\_0\_r> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <rx\_pcs\_reset\_1\_r> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <rx\_pcs\_reset\_0\_r> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rx\_client\_clk\_out\_1\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rx\_client\_clk\_out\_0\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <gtx\_clk\_ibufg\_1\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <gtx\_clk\_ibufg\_0\_i> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Found 4-bit register for signal <reset\_r>.

Summary:

inferred 4 D-type flip-flop(s).

Unit <ethmac\_v1\_8\_block> synthesized.

Synthesizing Unit <ethmac\_v1\_8\_locallink>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_locallink.v".

Found 1-bit register for signal <rx\_bad\_frame\_0\_r>.

Found 1-bit register for signal <rx\_bad\_frame\_1\_r>.

Found 8-bit register for signal <rx\_data\_0\_r>.

Found 8-bit register for signal <rx\_data\_1\_r>.

Found 1-bit register for signal <rx\_data\_valid\_0\_r>.

Found 1-bit register for signal <rx\_data\_valid\_1\_r>.

Found 1-bit register for signal <rx\_good\_frame\_0\_r>.

Found 1-bit register for signal <rx\_good\_frame\_1\_r>.

Found 6-bit register for signal <rx\_pre\_reset\_0\_i>.

Found 6-bit register for signal <rx\_pre\_reset\_1\_i>.

Found 1-bit register for signal <rx\_reset\_0\_i>.

Found 1-bit register for signal <rx\_reset\_1\_i>.

Found 6-bit register for signal <tx\_pre\_reset\_0\_i>.

Found 6-bit register for signal <tx\_pre\_reset\_1\_i>.

Found 1-bit register for signal <tx\_reset\_0\_i>.

Found 1-bit register for signal <tx\_reset\_1\_i>.

Summary:

inferred 50 D-type flip-flop(s).

Unit <ethmac\_v1\_8\_locallink> synthesized.

Synthesizing Unit <ethmac\_v1\_8\_design>.

Related source file is "\_rtl/ethmac\_v1\_8/example\_design/ethmac\_v1\_8\_design.v".

WARNING:Xst:647 - Input <CLK125\_DS> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:1780 - Signal <tx\_ll\_src\_rdy\_n\_1\_i> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <tx\_ll\_src\_rdy\_n\_0\_i> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <tx\_ll\_sof\_n\_1\_i> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <tx\_ll\_sof\_n\_0\_i> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <tx\_ll\_eof\_n\_1\_i> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <tx\_ll\_eof\_n\_0\_i> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <tx\_ll\_dst\_rdy\_n\_1\_i> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <tx\_ll\_dst\_rdy\_n\_0\_i> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <tx\_ll\_data\_1\_i> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:1780 - Signal <tx\_ll\_data\_0\_i> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:653 - Signal <HOSTWRDATA> is used but never assigned. This sourceless signal will be automatically connected to value 00000000000000000000000000000000.

WARNING:Xst:653 - Signal <HOSTREQ> is used but never assigned. This sourceless signal will be automatically connected to value 0.

WARNING:Xst:646 - Signal <HOSTRDDATA> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:653 - Signal <HOSTOPCODE> is used but never assigned. This sourceless signal will be automatically connected to value 00.

WARNING:Xst:653 - Signal <HOSTMIIMSEL> is used but never assigned. This sourceless signal will be automatically connected to value 0.

WARNING:Xst:646 - Signal <HOSTMIIMRDY> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:653 - Signal <HOSTEMAC1SEL> is used but never assigned. This sourceless signal will be automatically connected to value 0.

WARNING:Xst:653 - Signal <HOSTADDR> is used but never assigned. This sourceless signal will be automatically connected to value 0000000000.

Found 6-bit register for signal <ll\_pre\_reset\_0\_i>.

Found 6-bit register for signal <ll\_pre\_reset\_1\_i>.

Found 1-bit register for signal <ll\_reset\_0\_i>.

Found 1-bit register for signal <ll\_reset\_1\_i>.

Found 4-bit register for signal <reset\_r>.

Summary:

inferred 18 D-type flip-flop(s).

Unit <ethmac\_v1\_8\_design> synthesized.

Synthesizing Unit <topMain>.

Related source file is "topMain.vf".

WARNING:Xst:653 - Signal <tx\_src\_rdy\_0> is used but never assigned. This sourceless signal will be automatically connected to value 0.

WARNING:Xst:653 - Signal <tx\_sof\_0> is used but never assigned. This sourceless signal will be automatically connected to value 0.

WARNING:Xst:653 - Signal <tx\_eof\_0> is used but never assigned. This sourceless signal will be automatically connected to value 0.

WARNING:Xst:646 - Signal <tx\_dst\_rdy\_0> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:653 - Signal <tx\_data\_0> is used but never assigned. This sourceless signal will be automatically connected to value 00000000.

WARNING:Xst:646 - Signal <rx\_ll\_src\_rdy\_0> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rx\_ll\_sof\_0> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rx\_ll\_eof\_0> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <rx\_ll\_data\_0> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:653 - Signal <XLXN\_48> is used but never assigned. This sourceless signal will be automatically connected to value 0.

Unit <topMain> synthesized.

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic operations in this design can share the same physical resources for reduced device utilization. For improved clock frequency you may try to disable resource sharing.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 30

10-bit adder : 1

11-bit adder : 1

12-bit adder : 4

12-bit subtractor : 8

16-bit adder : 2

16-bit subtractor : 1

3-bit adder : 1

32-bit adder : 3

4-bit adder : 1

4-bit subtractor : 3

5-bit adder : 3

9-bit adder : 2

# Counters : 21

10-bit up counter : 3

11-bit up counter : 2

12-bit up counter : 4

32-bit up counter : 3

4-bit up counter : 2

8-bit down counter : 1

9-bit up counter : 2

9-bit updown counter : 4

# Accumulators : 2

12-bit updown accumulator : 2

# Registers : 382

1-bit register : 288

10-bit register : 1

11-bit register : 1

12-bit register : 24

16-bit register : 3

3-bit register : 4

32-bit register : 5

4-bit register : 4

5-bit register : 4

8-bit register : 48

# Comparators : 22

16-bit comparator greatequal : 2

16-bit comparator less : 2

16-bit comparator lessequal : 1

5-bit comparator lessequal : 3

8-bit comparator equal : 12

9-bit comparator greater : 2

# Multiplexers : 3

1-bit 8-to-1 multiplexer : 2

32-bit 7-to-1 multiplexer : 1

# Xors : 52

1-bit xor2 : 52

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

Analyzing FSM <FSM\_13> for best encoding.

Optimizing FSM <XLXI\_14/cstate/FSM> on signal <cstate[1:81]> with one-hot encoding.

-----------------------------------------------------------------------------------------------

State | Encoding

-----------------------------------------------------------------------------------------------

00000000 | 000000000000000000000000000000000000000000000000000000000000000000000000000000001

00000001 | 000000000000000000000000000000000000000000000000000000000000000000000000000000010

00000010 | 000000000000000000000000000000000000000000000000000000000000000000000000000000100

00000011 | 000000000000000000000000000000000000000000000000000000000000000000000000000001000

00000100 | 000000000000000000000000000000000000000000000000000000000000000000000000000010000

00000101 | 000000000000000000000000000000000000000000000000000000000000000000000000000100000

00000110 | 000000000000000000000000000000000000000000000000000000000000000000000000001000000

00000111 | 000000000000000000000000000000000000000000000000000000000000000000000000010000000

00001000 | 000000000000000000000000000000000000000000000000000000000000000000000000100000000

00001001 | 000000000000000000000000000000000000000000000000000000000000000000000001000000000

00001010 | 000000000000000000000000000000000000000000000000000000000000000000000010000000000

00001011 | 000000000000000000000000000000000000000000000000000000000000000000000100000000000

00001100 | 000000000000000000000000000000000000000000000000000000000000000000001000000000000

00001101 | 000000000000000000000000000000000000000000000000000000000000000000010000000000000

00001110 | 000000000000000000000000000000000000000000000000000000000000000000100000000000000

00001111 | 000000000000000000000000000000000000000000000000000000000000000001000000000000000

00010000 | 000000000000000000000000000000000000000000000000000000000000000010000000000000000

00010001 | 000000000000000000000000000000000000000000000000000000000000000100000000000000000

00010010 | 000000000000000000000000000000000000000000000000000000000000001000000000000000000

00010011 | 000000000000000000000000000000000000000000000000000000000000010000000000000000000

00010100 | 000000000000000000000000000000000000000000000000000000000001000000000000000000000

00010101 | 000000000000000000000000000000000000000000000000000000000010000000000000000000000

00010110 | 000000000000000000000000000000000000000000000000000000000100000000000000000000000

00010111 | 000000000000000000000000000000000000000000000000000000001000000000000000000000000

00011000 | 000000000000000000000000000000000000000000000000000000010000000000000000000000000

00011001 | 000000000000000000000000000000000000000000000000000000100000000000000000000000000

00011010 | 000000000000000000000000000000000000000000000000000001000000000000000000000000000

00011011 | 000000000000000000000000000000000000000000000000000010000000000000000000000000000

00011100 | 000000000000000000000000000000000000000000000000000100000000000000000000000000000

00011101 | 000000000000000000000000000000000000000000000000001000000000000000000000000000000

00011110 | 000000000000000000000000000000000000000000000000010000000000000000000000000000000

00011111 | 000000000000000000000000000000000000000000000000100000000000000000000000000000000

00100000 | 000000000000000000000000000000000000000000000001000000000000000000000000000000000

00100001 | 000000000000000000000000000000000000000000000010000000000000000000000000000000000

00100010 | 000000000000000000000000000000000000000000000100000000000000000000000000000000000

00100011 | 000000000000000000000000000000000000000000001000000000000000000000000000000000000

00100100 | 000000000000000000000000000000000000000000010000000000000000000000000000000000000

00100101 | 000000000000000000000000000000000000000000100000000000000000000000000000000000000

00100110 | 000000000000000000000000000000000000000001000000000000000000000000000000000000000

00100111 | 000000000000000000000000000000000000000010000000000000000000000000000000000000000

00101000 | 000000000000000000000000000000000000000100000000000000000000000000000000000000000

00101001 | 000000000000000000000000000000000000001000000000000000000000000000000000000000000

00101010 | 000000000000000000000000000000000000010000000000000000000000000000000000000000000

00101011 | 000000000000000000000000000000000000100000000000000000000000000000000000000000000

00101100 | 000000000000000000000000000000000001000000000000000000000000000000000000000000000

00101101 | 000000000000000000000000000000000010000000000000000000000000000000000000000000000

00101110 | 000000000000000000000000000000000100000000000000000000000000000000000000000000000

00101111 | 000000000000000000000000000000001000000000000000000000000000000000000000000000000

00110000 | 000000000000000000000000000000010000000000000000000000000000000000000000000000000

00110001 | 000000000000000000000000000000100000000000000000000000000000000000000000000000000

00110010 | 000000000000000000000000000001000000000000000000000000000000000000000000000000000

00110011 | 000000000000000000000000000010000000000000000000000000000000000000000000000000000

00110100 | 000000000000000000000000000100000000000000000000000000000000000000000000000000000

00110101 | 000000000000000000000000001000000000000000000000000000000000000000000000000000000

00110110 | 000000000000000000000000010000000000000000000000000000000000000000000000000000000

00110111 | 000000000000000000000000100000000000000000000000000000000000000000000000000000000

00111000 | 000000000000000000000001000000000000000000000000000000000000000000000000000000000

00111001 | 000000000000000000000010000000000000000000000000000000000000000000000000000000000

00111010 | 000000000000000000000100000000000000000000000000000000000000000000000000000000000

00111011 | 000000000000000000001000000000000000000000000000000000000000000000000000000000000

00111100 | 000000000000000000010000000000000000000000000000000000000000000000000000000000000

00111101 | 000000000000000000100000000000000000000000000000000000000000000000000000000000000

00111110 | 000000000000000001000000000000000000000000000000000000000000000000000000000000000

00111111 | 000000000000000000000000000000000000000000000000000000000000100000000000000000000

01000000 | 000000000000000010000000000000000000000000000000000000000000000000000000000000000

01000001 | 000000000000000100000000000000000000000000000000000000000000000000000000000000000

01000010 | 000000000000001000000000000000000000000000000000000000000000000000000000000000000

01000011 | 000000000000010000000000000000000000000000000000000000000000000000000000000000000

01000100 | 000000000000100000000000000000000000000000000000000000000000000000000000000000000

01000101 | 000000000001000000000000000000000000000000000000000000000000000000000000000000000

01000110 | 000000000010000000000000000000000000000000000000000000000000000000000000000000000

01000111 | 000000000100000000000000000000000000000000000000000000000000000000000000000000000

01001000 | 000000001000000000000000000000000000000000000000000000000000000000000000000000000

01001001 | 000000010000000000000000000000000000000000000000000000000000000000000000000000000

01001010 | 000000100000000000000000000000000000000000000000000000000000000000000000000000000

01001011 | 000001000000000000000000000000000000000000000000000000000000000000000000000000000

01001100 | 000010000000000000000000000000000000000000000000000000000000000000000000000000000

01001101 | 000100000000000000000000000000000000000000000000000000000000000000000000000000000

01001110 | 001000000000000000000000000000000000000000000000000000000000000000000000000000000

01001111 | 010000000000000000000000000000000000000000000000000000000000000000000000000000000

01010000 | 100000000000000000000000000000000000000000000000000000000000000000000000000000000

-----------------------------------------------------------------------------------------------

Analyzing FSM <FSM\_12> for best encoding.

Optimizing FSM <XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac1/rx\_fifo\_i/wr\_state/FSM> on signal <wr\_state[1:3]> with gray encoding.

-------------------

State | Encoding

-------------------

000 | 000

001 | 001

010 | 111

011 | 010

100 | 110

101 | 011

-------------------

Analyzing FSM <FSM\_11> for best encoding.

Optimizing FSM <XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac1/rx\_fifo\_i/rd\_state/FSM> on signal <rd\_state[1:8]> with one-hot encoding.

-------------------

State | Encoding

-------------------

000 | 00000001

001 | 00000010

010 | 00000100

011 | 00001000

100 | 00010000

101 | 01000000

110 | 00100000

111 | 10000000

-------------------

Analyzing FSM <FSM\_10> for best encoding.

Optimizing FSM <XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac1/tx\_fifo\_i/rd\_state/FSM> on signal <rd\_state[1:9]> with one-hot encoding.

--------------------

State | Encoding

--------------------

0000 | 000000001

0001 | 000000100

0010 | 000001000

0011 | 000010000

0100 | 000100000

0101 | 001000000

0110 | 010000000

0111 | 100000000

1000 | 000000010

--------------------

Analyzing FSM <FSM\_9> for best encoding.

Optimizing FSM <XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac1/tx\_fifo\_i/wr\_state/FSM> on signal <wr\_state[1:2]> with user encoding.

-------------------

State | Encoding

-------------------

00 | 00

01 | 01

10 | 10

11 | 11

-------------------

Analyzing FSM <FSM\_8> for best encoding.

Optimizing FSM <XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac0/rx\_fifo\_i/wr\_state/FSM> on signal <wr\_state[1:3]> with gray encoding.

-------------------

State | Encoding

-------------------

000 | 000

001 | 001

010 | 111

011 | 010

100 | 110

101 | 011

-------------------

Analyzing FSM <FSM\_7> for best encoding.

Optimizing FSM <XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac0/rx\_fifo\_i/rd\_state/FSM> on signal <rd\_state[1:8]> with one-hot encoding.

-------------------

State | Encoding

-------------------

000 | 00000001

001 | 00000010

010 | 00000100

011 | 00001000

100 | 00010000

101 | 01000000

110 | 00100000

111 | 10000000

-------------------

Analyzing FSM <FSM\_6> for best encoding.

Optimizing FSM <XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac0/tx\_fifo\_i/rd\_state/FSM> on signal <rd\_state[1:9]> with one-hot encoding.

--------------------

State | Encoding

--------------------

0000 | 000000001

0001 | 000000100

0010 | 000001000

0011 | 000010000

0100 | 000100000

0101 | 001000000

0110 | 010000000

0111 | 100000000

1000 | 000000010

--------------------

Analyzing FSM <FSM\_5> for best encoding.

Optimizing FSM <XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac0/tx\_fifo\_i/wr\_state/FSM> on signal <wr\_state[1:2]> with user encoding.

-------------------

State | Encoding

-------------------

00 | 00

01 | 01

10 | 10

11 | 11

-------------------

Analyzing FSM <FSM\_4> for best encoding.

Optimizing FSM <XLXI\_12/st\_flash\_op/FSM> on signal <st\_flash\_op[1:27]> with one-hot encoding.

---------------------------------------

State | Encoding

---------------------------------------

000000 | 000000000000000000000000001

000001 | 000000000000000000000000010

000010 | 000000000000000000000000100

000011 | 000000000000000000000001000

000100 | 000000000000000000000010000

000101 | 000000000000000000000100000

000110 | 000000000000000000001000000

000111 | 000000000000000000010000000

001000 | 000000000000000000100000000

001001 | 000000000000000001000000000

001010 | 000000000000000010000000000

001011 | 000000000000000100000000000

001100 | 000000000000001000000000000

001101 | 000000000000010000000000000

001110 | 000000000000100000000000000

001111 | 000000000001000000000000000

010000 | 000000000100000000000000000

010001 | 000000000010000000000000000

010010 | 000000010000000000000000000

010011 | 000000100000000000000000000

010100 | 000001000000000000000000000

010101 | 000010000000000000000000000

010110 | 000100000000000000000000000

010111 | 001000000000000000000000000

011000 | 010000000000000000000000000

011001 | 000000001000000000000000000

011010 | 100000000000000000000000000

---------------------------------------

Analyzing FSM <FSM\_3> for best encoding.

Optimizing FSM <XLXI\_12/st\_rx\_config/FSM> on signal <st\_rx\_config[1:19]> with one-hot encoding.

------------------------------

State | Encoding

------------------------------

00000 | 0000000000000000001

00001 | 0000000000000000010

00010 | 0000000000000000100

00011 | 0000000000000001000

00100 | 0000000000000010000

00101 | 0000000000000100000

00110 | 0000000000001000000

00111 | 0000000000010000000

01000 | 0000000000100000000

01001 | 0000000001000000000

01010 | 0000000010000000000

01011 | 0000000100000000000

01100 | 0000001000000000000

01101 | 0000010000000000000

01110 | 0000100000000000000

01111 | 0001000000000000000

10000 | 0010000000000000000

10001 | 0100000000000000000

11111 | 1000000000000000000

------------------------------

Analyzing FSM <FSM\_2> for best encoding.

Optimizing FSM <XLXI\_12/st\_wait\_sync/FSM> on signal <st\_wait\_sync[1:3]> with user encoding.

-------------------

State | Encoding

-------------------

000 | 000

001 | 001

010 | 010

011 | 011

100 | 100

-------------------

Analyzing FSM <FSM\_1> for best encoding.

Optimizing FSM <XLXI\_1/uut\_rx\_0/cstate/FSM> on signal <cstate[1:2]> with gray encoding.

Optimizing FSM <XLXI\_1/uut\_rx\_1/cstate/FSM> on signal <cstate[1:2]> with gray encoding.

-------------------

State | Encoding

-------------------

00000 | 00

00001 | 01

00010 | 11

00011 | 10

-------------------

Analyzing FSM <FSM\_0> for best encoding.

Optimizing FSM <XLXI\_13/cstate/FSM> on signal <cstate[1:4]> with gray encoding.

------------------------------

State | Encoding

------------------------------

0000000000000000 | 0000

0000000000000001 | 0001

0000000000000010 | 0011

0000000000000100 | 0010

0000000000001000 | 0110

0000000000010000 | 0111

0000000000100000 | 0101

0000000001000000 | 0100

0000000010000000 | 1100

0000000100000000 | 1101

0000001000000000 | 1111

0000010000000000 | 1110

0000100000000000 | 1010

0001000000000000 | 1011

0010000000000000 | 1001

0100000000000000 | 1000

------------------------------

WARNING:Xst:638 - in unit user\_spi\_flash\_ctrl Conflict on KEEP property on signal tx\_ll\_data<7> and tx\_ll\_data<6> tx\_ll\_data<6> signal will be lost.

WARNING:Xst:638 - in unit user\_spi\_flash\_ctrl Conflict on KEEP property on signal tx\_ll\_data<6> and tx\_ll\_data<5> tx\_ll\_data<5> signal will be lost.

WARNING:Xst:638 - in unit user\_spi\_flash\_ctrl Conflict on KEEP property on signal tx\_ll\_data<5> and tx\_ll\_data<4> tx\_ll\_data<4> signal will be lost.

WARNING:Xst:638 - in unit user\_spi\_flash\_ctrl Conflict on KEEP property on signal tx\_ll\_data<4> and tx\_ll\_data<3> tx\_ll\_data<3> signal will be lost.

WARNING:Xst:638 - in unit user\_spi\_flash\_ctrl Conflict on KEEP property on signal tx\_ll\_data<3> and tx\_ll\_data<2> tx\_ll\_data<2> signal will be lost.

WARNING:Xst:638 - in unit user\_spi\_flash\_ctrl Conflict on KEEP property on signal tx\_ll\_data<2> and tx\_ll\_data<1> tx\_ll\_data<1> signal will be lost.

WARNING:Xst:638 - in unit user\_spi\_flash\_ctrl Conflict on KEEP property on signal tx\_ll\_data<1> and tx\_ll\_data<0> tx\_ll\_data<0> signal will be lost.

WARNING:Xst:638 - in unit user\_spi\_flash\_ctrl Conflict on KEEP property on signal pp\_cycle\_tim and tx\_ll\_src\_rdy tx\_ll\_src\_rdy signal will be lost.

WARNING:Xst:638 - in unit user\_spi\_flash\_ctrl Conflict on KEEP property on signal pp\_cycle\_tim and tx\_ll\_eof tx\_ll\_eof signal will be lost.

WARNING:Xst:638 - in unit user\_spi\_flash\_ctrl Conflict on KEEP property on signal pp\_cycle\_tim and tx\_ll\_sof tx\_ll\_sof signal will be lost.

Reading core <ipcore\_dir/dualPortRAM.ngc>.

Loading core <dualPortRAM> for timing and area information for instance <uut\_dualportRAM>.

INFO:Xst:2261 - The FF/Latch <wr\_sof\_pipe\_0> in Unit <tx\_fifo\_i> is equivalent to the following FF/Latch, which will be removed : <wr\_eof\_pipe\_0>

INFO:Xst:2261 - The FF/Latch <wr\_sof\_pipe\_1> in Unit <tx\_fifo\_i> is equivalent to the following FF/Latch, which will be removed : <wr\_eof\_pipe\_1>

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_0\_i\_0> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_0\_i\_0>

WARNING:Xst:638 - in unit XLXI\_1/v5\_emac\_ll Conflict on KEEP property on signal tx\_pre\_reset\_0\_i<0> and rx\_pre\_reset\_0\_i<0> rx\_pre\_reset\_0\_i<0> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_1\_i\_0> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_1\_i\_0>

WARNING:Xst:638 - in unit XLXI\_1/v5\_emac\_ll Conflict on KEEP property on signal tx\_pre\_reset\_1\_i<0> and rx\_pre\_reset\_1\_i<0> rx\_pre\_reset\_1\_i<0> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_1\_i\_1> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_1\_i\_1>

WARNING:Xst:638 - in unit XLXI\_1/v5\_emac\_ll Conflict on KEEP property on signal tx\_pre\_reset\_1\_i<1> and rx\_pre\_reset\_1\_i<1> rx\_pre\_reset\_1\_i<1> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_0\_i\_1> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_0\_i\_1>

WARNING:Xst:638 - in unit XLXI\_1/v5\_emac\_ll Conflict on KEEP property on signal tx\_pre\_reset\_0\_i<1> and rx\_pre\_reset\_0\_i<1> rx\_pre\_reset\_0\_i<1> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_1\_i\_2> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_1\_i\_2>

WARNING:Xst:638 - in unit XLXI\_1/v5\_emac\_ll Conflict on KEEP property on signal tx\_pre\_reset\_1\_i<2> and rx\_pre\_reset\_1\_i<2> rx\_pre\_reset\_1\_i<2> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_0\_i\_2> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_0\_i\_2>

WARNING:Xst:638 - in unit XLXI\_1/v5\_emac\_ll Conflict on KEEP property on signal tx\_pre\_reset\_0\_i<2> and rx\_pre\_reset\_0\_i<2> rx\_pre\_reset\_0\_i<2> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_1\_i\_3> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_1\_i\_3>

WARNING:Xst:638 - in unit XLXI\_1/v5\_emac\_ll Conflict on KEEP property on signal tx\_pre\_reset\_1\_i<3> and rx\_pre\_reset\_1\_i<3> rx\_pre\_reset\_1\_i<3> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_0\_i\_3> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_0\_i\_3>

WARNING:Xst:638 - in unit XLXI\_1/v5\_emac\_ll Conflict on KEEP property on signal tx\_pre\_reset\_0\_i<3> and rx\_pre\_reset\_0\_i<3> rx\_pre\_reset\_0\_i<3> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_0\_i\_4> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_0\_i\_4>

WARNING:Xst:638 - in unit XLXI\_1/v5\_emac\_ll Conflict on KEEP property on signal tx\_pre\_reset\_0\_i<4> and rx\_pre\_reset\_0\_i<4> rx\_pre\_reset\_0\_i<4> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_1\_i\_4> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_1\_i\_4>

WARNING:Xst:638 - in unit XLXI\_1/v5\_emac\_ll Conflict on KEEP property on signal tx\_pre\_reset\_1\_i<4> and rx\_pre\_reset\_1\_i<4> rx\_pre\_reset\_1\_i<4> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_1\_i\_5> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_1\_i\_5>

WARNING:Xst:638 - in unit XLXI\_1/v5\_emac\_ll Conflict on KEEP property on signal tx\_pre\_reset\_1\_i<5> and rx\_pre\_reset\_1\_i<5> rx\_pre\_reset\_1\_i<5> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_0\_i\_5> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_0\_i\_5>

WARNING:Xst:638 - in unit XLXI\_1/v5\_emac\_ll Conflict on KEEP property on signal tx\_pre\_reset\_0\_i<5> and rx\_pre\_reset\_0\_i<5> rx\_pre\_reset\_0\_i<5> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_reset\_1\_i> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_reset\_1\_i>

INFO:Xst:2261 - The FF/Latch <tx\_reset\_0\_i> in Unit <v5\_emac\_ll> is equivalent to the following FF/Latch, which will be removed : <rx\_reset\_0\_i>

WARNING:Xst:1710 - FF/Latch <15> (without init value) has a constant value of 0 in block <data\_length>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <14> (without init value) has a constant value of 0 in block <data\_length>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <13> (without init value) has a constant value of 0 in block <data\_length>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <12> (without init value) has a constant value of 0 in block <data\_length>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <11> (without init value) has a constant value of 0 in block <data\_length>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <10> (without init value) has a constant value of 0 in block <data\_length>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <9> (without init value) has a constant value of 0 in block <data\_length>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <8> (without init value) has a constant value of 0 in block <data\_length>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <7> (without init value) has a constant value of 0 in block <data\_length>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <6> (without init value) has a constant value of 0 in block <data\_length>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <5> (without init value) has a constant value of 1 in block <data\_length>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <1> (without init value) has a constant value of 1 in block <data\_length>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <0> (without init value) has a constant value of 0 in block <data\_length>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <rd\_enable\_delay> (without init value) has a constant value of 1 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <rd\_enable\_delay> (without init value) has a constant value of 1 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_0> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_1> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_2> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_3> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_4> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_5> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_6> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_7> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_sof\_pipe\_0> (without init value) has a constant value of 1 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <rd\_enable\_delay2> (without init value) has a constant value of 1 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_0> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_1> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <rd\_enable\_delay2> (without init value) has a constant value of 1 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_2> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_sof\_pipe\_1> (without init value) has a constant value of 1 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_7> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_6> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_5> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_4> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_3> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_7> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_6> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_5> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_4> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_3> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_2> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_1> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_0> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_0> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_1> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <rd\_valid\_pipe\_2> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_0> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_1> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_0> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_1> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <rd\_valid\_pipe\_2> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_0> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_1> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:1710 - FF/Latch <wr\_eof\_bram\_0> (without init value) has a constant value of 1 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

Synthesizing (advanced) Unit <tx\_client\_fifo\_8\_1>.

INFO:Xst:2774 - HDL ADVISOR - ASYNC\_REG property attached to signal wr\_rd\_addr may hinder XST clustering optimizations.

Unit <tx\_client\_fifo\_8\_1> synthesized (advanced).

Synthesizing (advanced) Unit <tx\_client\_fifo\_8\_2>.

INFO:Xst:2774 - HDL ADVISOR - ASYNC\_REG property attached to signal wr\_rd\_addr may hinder XST clustering optimizations.

Unit <tx\_client\_fifo\_8\_2> synthesized (advanced).

Synthesizing (advanced) Unit <user\_spi\_flash\_ctrl>.

INFO:Xst:2774 - HDL ADVISOR - KEEP property attached to signal tx\_bit\_cnt may hinder XST clustering optimizations.

INFO:Xst:2774 - HDL ADVISOR - KEEP property attached to signal wait\_be\_done\_cnt may hinder XST clustering optimizations.

INFO:Xst:2774 - HDL ADVISOR - KEEP property attached to signal wait\_data\_cnt may hinder XST clustering optimizations.

Unit <user\_spi\_flash\_ctrl> synthesized (advanced).

WARNING:Xst:2677 - Node <rd\_valid\_pipe\_2> of sequential type is unconnected in block <rx\_client\_fifo\_8\_1>.

WARNING:Xst:2677 - Node <rd\_valid\_pipe\_2> of sequential type is unconnected in block <rx\_client\_fifo\_8\_2>.

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Advanced HDL Synthesis Report

Macro Statistics

# FSMs : 14

# Adders/Subtractors : 30

10-bit adder : 1

11-bit adder : 1

12-bit adder : 4

12-bit subtractor : 8

16-bit adder : 2

16-bit subtractor : 1

3-bit adder : 2

3-bit subtractor : 2

32-bit adder : 3

4-bit subtractor : 1

5-bit adder : 3

9-bit adder : 2

# Counters : 21

10-bit up counter : 3

11-bit up counter : 2

12-bit up counter : 4

32-bit up counter : 3

4-bit up counter : 2

8-bit down counter : 1

9-bit up counter : 2

9-bit updown counter : 4

# Accumulators : 2

12-bit updown accumulator : 2

# Registers : 1235

Flip-Flops : 1235

# Comparators : 22

16-bit comparator greatequal : 2

16-bit comparator less : 2

16-bit comparator lessequal : 1

5-bit comparator lessequal : 3

8-bit comparator equal : 12

9-bit comparator greater : 2

# Multiplexers : 3

1-bit 8-to-1 multiplexer : 2

32-bit 7-to-1 multiplexer : 1

# Xors : 52

1-bit xor2 : 52

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\* Low Level Synthesis \*

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WARNING:Xst:1710 - FF/Latch <rd\_enable\_delay> (without init value) has a constant value of 1 in block <tx\_client\_fifo\_8\_1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <rd\_enable\_delay2> (without init value) has a constant value of 1 in block <tx\_client\_fifo\_8\_1>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <rd\_enable\_delay> (without init value) has a constant value of 1 in block <tx\_client\_fifo\_8\_2>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <rd\_enable\_delay2> (without init value) has a constant value of 1 in block <tx\_client\_fifo\_8\_2>. This FF/Latch will be trimmed during the optimization process.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_0\_i\_0> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_0\_i\_0>

WARNING:Xst:638 - in unit ethmac\_v1\_8\_locallink Conflict on KEEP property on signal tx\_pre\_reset\_0\_i<0> and rx\_pre\_reset\_0\_i<0> rx\_pre\_reset\_0\_i<0> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_1\_i\_0> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_1\_i\_0>

WARNING:Xst:638 - in unit ethmac\_v1\_8\_locallink Conflict on KEEP property on signal tx\_pre\_reset\_1\_i<0> and rx\_pre\_reset\_1\_i<0> rx\_pre\_reset\_1\_i<0> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_1\_i\_1> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_1\_i\_1>

WARNING:Xst:638 - in unit ethmac\_v1\_8\_locallink Conflict on KEEP property on signal tx\_pre\_reset\_1\_i<1> and rx\_pre\_reset\_1\_i<1> rx\_pre\_reset\_1\_i<1> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_0\_i\_1> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_0\_i\_1>

WARNING:Xst:638 - in unit ethmac\_v1\_8\_locallink Conflict on KEEP property on signal tx\_pre\_reset\_0\_i<1> and rx\_pre\_reset\_0\_i<1> rx\_pre\_reset\_0\_i<1> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_1\_i\_2> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_1\_i\_2>

WARNING:Xst:638 - in unit ethmac\_v1\_8\_locallink Conflict on KEEP property on signal tx\_pre\_reset\_1\_i<2> and rx\_pre\_reset\_1\_i<2> rx\_pre\_reset\_1\_i<2> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_0\_i\_2> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_0\_i\_2>

WARNING:Xst:638 - in unit ethmac\_v1\_8\_locallink Conflict on KEEP property on signal tx\_pre\_reset\_0\_i<2> and rx\_pre\_reset\_0\_i<2> rx\_pre\_reset\_0\_i<2> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_1\_i\_3> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_1\_i\_3>

WARNING:Xst:638 - in unit ethmac\_v1\_8\_locallink Conflict on KEEP property on signal tx\_pre\_reset\_1\_i<3> and rx\_pre\_reset\_1\_i<3> rx\_pre\_reset\_1\_i<3> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_0\_i\_3> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_0\_i\_3>

WARNING:Xst:638 - in unit ethmac\_v1\_8\_locallink Conflict on KEEP property on signal tx\_pre\_reset\_0\_i<3> and rx\_pre\_reset\_0\_i<3> rx\_pre\_reset\_0\_i<3> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_0\_i\_4> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_0\_i\_4>

WARNING:Xst:638 - in unit ethmac\_v1\_8\_locallink Conflict on KEEP property on signal tx\_pre\_reset\_0\_i<4> and rx\_pre\_reset\_0\_i<4> rx\_pre\_reset\_0\_i<4> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_1\_i\_4> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_1\_i\_4>

WARNING:Xst:638 - in unit ethmac\_v1\_8\_locallink Conflict on KEEP property on signal tx\_pre\_reset\_1\_i<4> and rx\_pre\_reset\_1\_i<4> rx\_pre\_reset\_1\_i<4> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_1\_i\_5> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_1\_i\_5>

WARNING:Xst:638 - in unit ethmac\_v1\_8\_locallink Conflict on KEEP property on signal tx\_pre\_reset\_1\_i<5> and rx\_pre\_reset\_1\_i<5> rx\_pre\_reset\_1\_i<5> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_pre\_reset\_0\_i\_5> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_pre\_reset\_0\_i\_5>

WARNING:Xst:638 - in unit ethmac\_v1\_8\_locallink Conflict on KEEP property on signal tx\_pre\_reset\_0\_i<5> and rx\_pre\_reset\_0\_i<5> rx\_pre\_reset\_0\_i<5> signal will be lost.

INFO:Xst:2261 - The FF/Latch <tx\_reset\_1\_i> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_reset\_1\_i>

INFO:Xst:2261 - The FF/Latch <tx\_reset\_0\_i> in Unit <ethmac\_v1\_8\_locallink> is equivalent to the following FF/Latch, which will be removed : <rx\_reset\_0\_i>

WARNING:Xst:1710 - FF/Latch <wb\_dat\_o\_31> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_30> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_29> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_28> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_27> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_26> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_25> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_24> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_23> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_22> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_21> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_20> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_19> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_18> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_17> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_16> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_15> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wb\_dat\_o\_14> (without init value) has a constant value of 0 in block <spi\_top>. This FF/Latch will be trimmed during the optimization process.

INFO:Xst:1901 - Instance ramgen\_l in unit tx\_client\_fifo\_8\_1 of type RAMB16\_S9\_S9 has been replaced by RAMB16

INFO:Xst:1901 - Instance ramgen\_u in unit tx\_client\_fifo\_8\_1 of type RAMB16\_S9\_S9 has been replaced by RAMB16

INFO:Xst:1901 - Instance ramgen\_l in unit rx\_client\_fifo\_8\_1 of type RAMB16\_S9\_S9 has been replaced by RAMB16

INFO:Xst:1901 - Instance ramgen\_u in unit rx\_client\_fifo\_8\_1 of type RAMB16\_S9\_S9 has been replaced by RAMB16

INFO:Xst:1901 - Instance ramgen\_l in unit tx\_client\_fifo\_8\_2 of type RAMB16\_S9\_S9 has been replaced by RAMB16

INFO:Xst:1901 - Instance ramgen\_u in unit tx\_client\_fifo\_8\_2 of type RAMB16\_S9\_S9 has been replaced by RAMB16

INFO:Xst:1901 - Instance ramgen\_l in unit rx\_client\_fifo\_8\_2 of type RAMB16\_S9\_S9 has been replaced by RAMB16

INFO:Xst:1901 - Instance ramgen\_u in unit rx\_client\_fifo\_8\_2 of type RAMB16\_S9\_S9 has been replaced by RAMB16

INFO:Xst:1901 - Instance XLXI\_9 in unit topMain of type PLL\_BASE has been replaced by PLL\_ADV

WARNING:Xst:1710 - FF/Latch <data\_length\_15> (without init value) has a constant value of 0 in block <tx\_control>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data\_length\_14> (without init value) has a constant value of 0 in block <tx\_control>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data\_length\_13> (without init value) has a constant value of 0 in block <tx\_control>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data\_length\_12> (without init value) has a constant value of 0 in block <tx\_control>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data\_length\_11> (without init value) has a constant value of 0 in block <tx\_control>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data\_length\_10> (without init value) has a constant value of 0 in block <tx\_control>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data\_length\_9> (without init value) has a constant value of 0 in block <tx\_control>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data\_length\_8> (without init value) has a constant value of 0 in block <tx\_control>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data\_length\_7> (without init value) has a constant value of 0 in block <tx\_control>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data\_length\_6> (without init value) has a constant value of 0 in block <tx\_control>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data\_length\_5> (without init value) has a constant value of 1 in block <tx\_control>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data\_length\_1> (without init value) has a constant value of 1 in block <tx\_control>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data\_length\_0> (without init value) has a constant value of 0 in block <tx\_control>. This FF/Latch will be trimmed during the optimization process.

INFO:Xst:2261 - The FF/Latch <data\_length\_3> in Unit <tx\_control> is equivalent to the following FF/Latch, which will be removed : <data\_length\_2>

Optimizing unit <topMain> ...

Optimizing unit <Div\_Ctrl> ...

Optimizing unit <rx\_check> ...

Optimizing unit <spi\_clgen> ...

Optimizing unit <spi\_shift> ...

Optimizing unit <user\_spi\_flash\_ctrl> ...

Optimizing unit <ethmac\_v1\_8> ...

Optimizing unit <ROCKETIO\_WRAPPER\_GTP\_TILE> ...

Optimizing unit <tx\_client\_fifo\_8\_1> ...

Optimizing unit <rx\_client\_fifo\_8\_1> ...

Optimizing unit <tx\_client\_fifo\_8\_2> ...

Optimizing unit <rx\_client\_fifo\_8\_2> ...

Optimizing unit <tx\_control> ...

Optimizing unit <spi\_top> ...

Optimizing unit <eth\_fifo\_8\_1> ...

Optimizing unit <eth\_fifo\_8\_2> ...

Optimizing unit <ROCKETIO\_WRAPPER\_GTP> ...

Optimizing unit <m25pxx\_spi\_flash\_ctrl> ...

Optimizing unit <GTP\_dual\_1000X> ...

Optimizing unit <ethmac\_v1\_8\_block> ...

Optimizing unit <ethmac\_v1\_8\_locallink> ...

Optimizing unit <ethmac\_v1\_8\_design> ...

WARNING:Xst:1426 - The value init of the FF/Latch wr\_sof\_pipe\_0 hinder the constant cleaning in the block tx\_fifo\_i.

You should achieve better results by setting this init to 1.

WARNING:Xst:1426 - The value init of the FF/Latch wr\_eof\_pipe\_0 hinder the constant cleaning in the block tx\_fifo\_i.

You should achieve better results by setting this init to 1.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_0> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_1> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_2> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_3> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_4> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_5> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_6> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <wr\_data\_pipe\_0\_7> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_7> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_6> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_5> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_4> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_3> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_2> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_1> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_pipe\_1\_0> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_0> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_1> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_2> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_3> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_4> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_5> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_6> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <wr\_data\_bram\_7> (without init value) has a constant value of 0 in block <tx\_fifo\_i>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_3> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_2> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_1> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_0> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_0> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_1> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <rd\_sof\_n> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_3> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_2> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_1> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_0> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_0> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_1> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_3> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_2> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_1> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_0> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_0> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_1> of sequential type is unconnected in block <tx\_fifo\_i>.

WARNING:Xst:2677 - Node <rd\_sof\_n> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_3> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_2> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_1> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_fifo\_status\_0> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_0> of sequential type is unconnected in block <rx\_fifo\_i>.

WARNING:Xst:2677 - Node <wr\_addr\_diff\_1> of sequential type is unconnected in block <rx\_fifo\_i>.

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block topMain, actual ratio is 4.

Final Macro Processing ...

Processing Unit <XLXI\_1> :

INFO:Xst:741 - HDL ADVISOR - A 7-bit shift register was found for signal <ll\_reset\_0\_i> and currently occupies 7 logic cells (3 slices). Removing the set/reset logic would take advantage of SRL32 (and derived) primitives and reduce this to 1 logic cells (1 slices). Evaluate if the set/reset can be removed for this simple shift register. The majority of simple pipeline structures do not need to be set/reset operationally.

INFO:Xst:741 - HDL ADVISOR - A 7-bit shift register was found for signal <ll\_reset\_1\_i> and currently occupies 7 logic cells (3 slices). Removing the set/reset logic would take advantage of SRL32 (and derived) primitives and reduce this to 1 logic cells (1 slices). Evaluate if the set/reset can be removed for this simple shift register. The majority of simple pipeline structures do not need to be set/reset operationally.

Unit <XLXI\_1> processed.

Processing Unit <rx\_fifo\_i> :

Found 2-bit shift register for signal <rd\_valid\_pipe\_1>.

Found 2-bit shift register for signal <wr\_gf\_pipe\_1>.

Found 2-bit shift register for signal <wr\_bf\_pipe\_1>.

Found 3-bit shift register for signal <wr\_data\_bram\_0>.

Found 3-bit shift register for signal <wr\_data\_bram\_1>.

Found 3-bit shift register for signal <wr\_data\_bram\_2>.

Found 3-bit shift register for signal <wr\_data\_bram\_3>.

Found 3-bit shift register for signal <wr\_data\_bram\_4>.

Found 3-bit shift register for signal <wr\_data\_bram\_5>.

Found 3-bit shift register for signal <wr\_data\_bram\_6>.

Found 3-bit shift register for signal <wr\_data\_bram\_7>.

Found 2-bit shift register for signal <rd\_valid\_pipe\_1>.

Found 2-bit shift register for signal <wr\_gf\_pipe\_1>.

Found 2-bit shift register for signal <wr\_bf\_pipe\_1>.

Found 3-bit shift register for signal <wr\_data\_bram\_0>.

Found 3-bit shift register for signal <wr\_data\_bram\_1>.

Found 3-bit shift register for signal <wr\_data\_bram\_2>.

Found 3-bit shift register for signal <wr\_data\_bram\_3>.

Found 3-bit shift register for signal <wr\_data\_bram\_4>.

Found 3-bit shift register for signal <wr\_data\_bram\_5>.

Found 3-bit shift register for signal <wr\_data\_bram\_6>.

Found 3-bit shift register for signal <wr\_data\_bram\_7>.

Unit <rx\_fifo\_i> processed.

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Final Register Report

Macro Statistics

# Registers : 1547

Flip-Flops : 1547

# Shift Registers : 22

2-bit shift register : 6

3-bit shift register : 16

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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=========================================================================

\* Final Report \*

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Clock Information:

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------------------------------------------------------------------------------------------------------------+-------------------------------------------------------------------------------------------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

------------------------------------------------------------------------------------------------------------+-------------------------------------------------------------------------------------------------------------+-------+

XLXN\_33 | BUFG | 471 |

XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/REFCLKOUT\_OUT | BUFG | 1131 |

XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/tied\_to\_ground\_i| NONE(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/gtp\_dual\_i)| 1 |

------------------------------------------------------------------------------------------------------------+-------------------------------------------------------------------------------------------------------------+-------+

INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources. Please use the buffer\_type constraint in order to insert these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:

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-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------+-------------------------------------------------------------------------------------------------------------+-------+

Control Signal | Buffer(FF name) | Load |

-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------+-------------------------------------------------------------------------------------------------------------+-------+

XLXI\_12/rst\_n\_inv(XLXI\_12/rst\_n\_inv681\_INV\_0:O) | NONE(XLXI\_12/ADDRH\_r\_0) | 311 |

XLXI\_14/cstate\_FSM\_Acst\_FSM\_inv(XLXI\_14/cstate\_FSM\_Acst\_FSM\_inv1\_INV\_0:O) | NONE(XLXI\_14/RW\_i\_0) | 263 |

XLXI\_2/rst\_n\_inv(XLXI\_2/rst\_n\_inv1\_INV\_0:O) | NONE(XLXI\_2/TIM\_0) | 100 |

XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/tied\_to\_ground\_i(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/XST\_GND:G) | NONE(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/gtp\_dual\_i)| 98 |

reset\_i(XLXI\_3:O) | NONE(XLXI\_1/ll\_pre\_reset\_0\_i\_0) | 91 |

XLXI\_1/ll\_reset\_0\_i(XLXI\_1/ll\_reset\_0\_i:Q) | NONE(XLXI\_1/uut\_rx\_0/ByteCnt\_0) | 25 |

XLXI\_1/ll\_reset\_1\_i(XLXI\_1/ll\_reset\_1\_i:Q) | NONE(XLXI\_1/uut\_rx\_1/ByteCnt\_0) | 25 |

XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/tied\_to\_ground\_vec\_i(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/XST\_VCC:P)| NONE(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/gtp\_dual\_i)| 12 |

XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/N0(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/XST\_GND:G) | NONE(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/gtp\_dual\_i)| 8 |

XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/POWERDOWN\_0(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/v5\_emac:EMAC0PHYPOWERDOWN) | NONE(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/gtp\_dual\_i)| 8 |

XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/POWERDOWN\_1(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/v5\_emac:EMAC1PHYPOWERDOWN) | NONE(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/gtp\_dual\_i)| 8 |

XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/MGTRXRESET\_0(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/v5\_emac:EMAC0PHYMGTRXRESET) | NONE(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/gtp\_dual\_i)| 4 |

XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/MGTRXRESET\_1(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/v5\_emac:EMAC1PHYMGTRXRESET) | NONE(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/gtp\_dual\_i)| 4 |

MGTREFCLKP | IBUFDS | 2 |

MGTRXN0 | IBUF | 2 |

MGTRXN1 | IBUF | 2 |

MGTRXP0 | IBUF | 2 |

MGTRXP1 | IBUF | 2 |

XLXI\_1/reset\_r<3>(XLXI\_1/reset\_r\_3:Q) | NONE(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/gtp\_dual\_i)| 2 |

XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/LOOPBACKMSB\_0(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/v5\_emac:EMAC0PHYLOOPBACKMSB) | NONE(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/gtp\_dual\_i)| 2 |

XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/LOOPBACKMSB\_1(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/v5\_emac:EMAC1PHYLOOPBACKMSB) | NONE(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/gtp\_dual\_i)| 2 |

XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/MGTTXRESET\_0(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/v5\_emac:EMAC0PHYMGTTXRESET) | NONE(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/gtp\_dual\_i)| 2 |

XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/MGTTXRESET\_1(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/v5\_emac\_wrapper\_inst/v5\_emac:EMAC1PHYMGTTXRESET) | NONE(XLXI\_1/v5\_emac\_ll/v5\_emac\_block\_inst/GTP\_DUAL\_1000X\_inst/GTP\_1000X/tile0\_rocketio\_wrapper\_i/gtp\_dual\_i)| 2 |

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Timing Summary:

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Speed Grade: -1

Minimum period: 4.717ns (Maximum Frequency: 211.999MHz)

Minimum input arrival time before clock: 5.274ns

Maximum output required time after clock: 5.717ns

Maximum combinational path delay: 2.019ns

=========================================================================

Process "Synthesize - XST" completed successfully

Started : "Translate".

Running inserter...

Command Line: inserter -intstyle ise -mode insert -ise\_project\_dir F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test -proj topmain.cdc -intstyle ise -dd F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/\_ngo -uc F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/topmain.ucf -sd ipcore\_dir -p xc5vlx30t-ff323-1 F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/topMain.ngc topMain\_cs.ngc

Release 13.3 ChipScope Core Inserter 13300.11.276.1137

Copyright (c) 1999-2011 Xilinx, Inc. All Rights Reserved.

Command Line: inserter -intstyle ise -mode insert -ise\_project\_dir F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test -proj topmain.cdc -intstyle ise -dd F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/\_ngo -uc F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/topmain.ucf -sd ipcore\_dir -p xc5vlx30t-ff323-1 F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/topMain.ngc topMain\_cs.ngc -server

ChipScope: Launching Server C:\Xilinx\13.3\ISE\_DS\ISE\bin\nt64\InserterServer.exe

Connecting to server output stream

Started ChipScope Core Insertion Operation

ngcbuild.exe -dd F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/\_ngo -sd ipcore\_dir -p xc5vlx30t-ff323-1 -i F:\fpgaWorks\flash\_iap\user\_config\_flash\_v\_30T\_test\topMain.ngc F:\fpgaWorks\flash\_iap\user\_config\_flash\_v\_30T\_test\topMain\_cs.ngc

Release 13.3 - ngcbuild O.76xd (nt64)

Copyright (c) 1995-2011 Xilinx, Inc. All rights reserved.

Command Line: ngcbuild.exe -dd

F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/\_ngo -sd ipcore\_dir -p

xc5vlx30t-ff323-1 -i

F:\fpgaWorks\flash\_iap\user\_config\_flash\_v\_30T\_test\topMain.ngc

F:\fpgaWorks\flash\_iap\user\_config\_flash\_v\_30T\_test\topMain\_cs.ngc

Reading NGO file

"F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/topMain.ngc" ...

Loading design module "ipcore\_dir/dualPortRAM.ngc"...

Partition Implementation Status

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No Partitions were found in this design.

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NGCBUILD Design Results Summary:

Number of errors: 0

Number of warnings: 0

Writing NGC file

"F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/topMain\_cs.ngc" ...

Total REAL time to NGCBUILD completion: 2 sec

Total CPU time to NGCBUILD completion: 2 sec

Writing NGCBUILD log file

"F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/topMain\_cs.blc"...

NGCBUILD done.

Loading CDC project F:\fpgaWorks\flash\_iap\user\_config\_flash\_v\_30T\_test\topmain.cdc

Successfully read project F:\fpgaWorks\flash\_iap\user\_config\_flash\_v\_30T\_test\topmain.cdc

copy F:\fpgaWorks\flash\_iap\user\_config\_flash\_v\_30T\_test\topMain\_cs.ngc => F:\fpgaWorks\flash\_iap\user\_config\_flash\_v\_30T\_test\\_ngo\topMain\_cs\_signalbrowser.ngo

Generating cores using CORE Generator. Please be patient as this can take several minutes...

Using existing cached core F:\fpgaWorks\flash\_iap\user\_config\_flash\_v\_30T\_test\\_ngo\cs\_icon\_pro\generate\_icon\_pro.xco

Using existing cached core F:\fpgaWorks\flash\_iap\user\_config\_flash\_v\_30T\_test\\_ngo\cs\_ila\_pro\_0\generate\_ila\_pro\_0.xco

Making net connections...

Writing Output Netlist F:\fpgaWorks\flash\_iap\user\_config\_flash\_v\_30T\_test\topMain\_cs.ngc...

Core Generation and Insertion Operations Complete.

Running ngdbuild...

Command Line: ngdbuild -intstyle ise -dd \_ngo -sd ipcore\_dir -nt timestamp -uc topmain.ucf -p xc5vlx30t-ff323-1 topMain\_cs.ngc topMain.ngd

Command Line: C:\Xilinx\13.3\ISE\_DS\ISE\bin\nt64\unwrapped\ngdbuild.exe

-intstyle ise -dd \_ngo -sd ipcore\_dir -nt timestamp -uc topmain.ucf -p

xc5vlx30t-ff323-1 topMain\_cs.ngc topMain.ngd

Reading NGO file

"F:/fpgaWorks/flash\_iap/user\_config\_flash\_v\_30T\_test/topMain\_cs.ngc" ...

Gathering constraint information from source properties...

Done.

Annotating constraints to design from ucf file "topmain.ucf" ...

Resolving constraint associations...

Checking Constraint Associations...

Done...

Checking expanded design ...

WARNING:NgdBuild:452 - logical net 'ila0\_data0<69>' has no driver

WARNING:NgdBuild:452 - logical net 'XLXI\_1/TX\_LL\_DST\_RDY\_N\_0' has no driver

WARNING:NgdBuild:452 - logical net 'XLXI\_1/rx\_ll\_sof\_n\_0\_i' has no driver

WARNING:NgdBuild:452 - logical net 'XLXI\_1/rx\_ll\_sof\_n\_1\_i' has no driver

WARNING:NgdBuild:452 - logical net 'XLXI\_1/v5\_emac\_ll/RX\_LL\_FIFO\_STATUS\_0<0>'

has no driver

WARNING:NgdBuild:452 - logical net 'XLXI\_1/v5\_emac\_ll/RX\_LL\_FIFO\_STATUS\_0<1>'

has no driver

WARNING:NgdBuild:452 - logical net 'XLXI\_1/v5\_emac\_ll/RX\_LL\_FIFO\_STATUS\_0<2>'

has no driver

WARNING:NgdBuild:452 - logical net 'XLXI\_1/v5\_emac\_ll/RX\_LL\_FIFO\_STATUS\_0<3>'

has no driver

WARNING:NgdBuild:452 - logical net 'XLXI\_1/v5\_emac\_ll/RX\_LL\_FIFO\_STATUS\_1<0>'

has no driver

WARNING:NgdBuild:452 - logical net 'XLXI\_1/v5\_emac\_ll/RX\_LL\_FIFO\_STATUS\_1<1>'

has no driver

WARNING:NgdBuild:452 - logical net 'XLXI\_1/v5\_emac\_ll/RX\_LL\_FIFO\_STATUS\_1<2>'

has no driver

WARNING:NgdBuild:452 - logical net 'XLXI\_1/v5\_emac\_ll/RX\_LL\_FIFO\_STATUS\_1<3>'

has no driver

WARNING:NgdBuild:452 - logical net

'XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac0/rx\_overflow' has no driver

WARNING:NgdBuild:452 - logical net

'XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac0/tx\_fifo\_status<0>' has no driver

WARNING:NgdBuild:452 - logical net

'XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac0/tx\_fifo\_status<1>' has no driver

WARNING:NgdBuild:452 - logical net

'XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac0/tx\_fifo\_status<2>' has no driver

WARNING:NgdBuild:452 - logical net

'XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac0/tx\_fifo\_status<3>' has no driver

WARNING:NgdBuild:452 - logical net

'XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac0/tx\_overflow' has no driver

WARNING:NgdBuild:452 - logical net

'XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac1/rx\_overflow' has no driver

WARNING:NgdBuild:452 - logical net

'XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac1/tx\_fifo\_status<0>' has no driver

WARNING:NgdBuild:452 - logical net

'XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac1/tx\_fifo\_status<1>' has no driver

WARNING:NgdBuild:452 - logical net

'XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac1/tx\_fifo\_status<2>' has no driver

WARNING:NgdBuild:452 - logical net

'XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac1/tx\_fifo\_status<3>' has no driver

WARNING:NgdBuild:452 - logical net

'XLXI\_1/v5\_emac\_ll/client\_side\_FIFO\_emac1/tx\_overflow' has no driver

Partition Implementation Status

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No Partitions were found in this design.

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NGDBUILD Design Results Summary:

Number of errors: 0

Number of warnings: 24

Writing NGD file "topMain.ngd" ...

Total REAL time to NGDBUILD completion: 5 sec

Total CPU time to NGDBUILD completion: 5 sec

Writing NGDBUILD log file "topMain.bld"...

NGDBUILD done.

Process "Translate" completed successfully

Started : "Map".

Running map...

Command Line: map -intstyle ise -p xc5vlx30t-ff323-1 -w -logic\_opt off -ol high -t 1 -register\_duplication off -global\_opt off -mt off -cm area -ir off -pr off -lc off -power off -o topMain\_map.ncd topMain.ngd topMain.pcf

Using target part "5vlx30tff323-1".

Mapping design into LUTs...

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[0].u\_

ramb36/U\_RAMB36

of frag REGCLKAU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[0].u\_

ramb36/U\_RAMB36\_REGCLKAU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[0].u\_

ramb36/U\_RAMB36

of frag REGCLKAL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[0].u\_

ramb36/U\_RAMB36\_REGCLKAL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[0].u\_

ramb36/U\_RAMB36

of frag REGCLKBU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[0].u\_

ramb36/U\_RAMB36\_REGCLKBU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[0].u\_

ramb36/U\_RAMB36

of frag REGCLKBL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[0].u\_

ramb36/U\_RAMB36\_REGCLKBL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[10].u

\_ramb36/U\_RAMB36

of frag REGCLKAU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[10].u

\_ramb36/U\_RAMB36\_REGCLKAU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[10].u

\_ramb36/U\_RAMB36

of frag REGCLKAL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[10].u

\_ramb36/U\_RAMB36\_REGCLKAL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[10].u

\_ramb36/U\_RAMB36

of frag REGCLKBU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[10].u

\_ramb36/U\_RAMB36\_REGCLKBU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[10].u

\_ramb36/U\_RAMB36

of frag REGCLKBL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[10].u

\_ramb36/U\_RAMB36\_REGCLKBL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[1].u\_

ramb36/U\_RAMB36

of frag REGCLKAU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[1].u\_

ramb36/U\_RAMB36\_REGCLKAU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[1].u\_

ramb36/U\_RAMB36

of frag REGCLKAL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[1].u\_

ramb36/U\_RAMB36\_REGCLKAL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[1].u\_

ramb36/U\_RAMB36

of frag REGCLKBU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[1].u\_

ramb36/U\_RAMB36\_REGCLKBU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[1].u\_

ramb36/U\_RAMB36

of frag REGCLKBL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[1].u\_

ramb36/U\_RAMB36\_REGCLKBL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[2].u\_

ramb36/U\_RAMB36

of frag REGCLKAU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[2].u\_

ramb36/U\_RAMB36\_REGCLKAU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[2].u\_

ramb36/U\_RAMB36

of frag REGCLKAL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[2].u\_

ramb36/U\_RAMB36\_REGCLKAL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[2].u\_

ramb36/U\_RAMB36

of frag REGCLKBU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[2].u\_

ramb36/U\_RAMB36\_REGCLKBU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[2].u\_

ramb36/U\_RAMB36

of frag REGCLKBL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[2].u\_

ramb36/U\_RAMB36\_REGCLKBL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[3].u\_

ramb36/U\_RAMB36

of frag REGCLKAU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[3].u\_

ramb36/U\_RAMB36\_REGCLKAU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[3].u\_

ramb36/U\_RAMB36

of frag REGCLKAL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[3].u\_

ramb36/U\_RAMB36\_REGCLKAL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[3].u\_

ramb36/U\_RAMB36

of frag REGCLKBU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[3].u\_

ramb36/U\_RAMB36\_REGCLKBU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[3].u\_

ramb36/U\_RAMB36

of frag REGCLKBL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[3].u\_

ramb36/U\_RAMB36\_REGCLKBL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[4].u\_

ramb36/U\_RAMB36

of frag REGCLKAU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[4].u\_

ramb36/U\_RAMB36\_REGCLKAU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[4].u\_

ramb36/U\_RAMB36

of frag REGCLKAL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[4].u\_

ramb36/U\_RAMB36\_REGCLKAL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[4].u\_

ramb36/U\_RAMB36

of frag REGCLKBU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[4].u\_

ramb36/U\_RAMB36\_REGCLKBU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[4].u\_

ramb36/U\_RAMB36

of frag REGCLKBL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[4].u\_

ramb36/U\_RAMB36\_REGCLKBL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[5].u\_

ramb36/U\_RAMB36

of frag REGCLKAU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[5].u\_

ramb36/U\_RAMB36\_REGCLKAU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[5].u\_

ramb36/U\_RAMB36

of frag REGCLKAL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[5].u\_

ramb36/U\_RAMB36\_REGCLKAL\_tiesig

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U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[5].u\_

ramb36/U\_RAMB36

of frag REGCLKBU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[5].u\_

ramb36/U\_RAMB36\_REGCLKBU\_tiesig

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U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[5].u\_

ramb36/U\_RAMB36

of frag REGCLKBL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[5].u\_

ramb36/U\_RAMB36\_REGCLKBL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[6].u\_

ramb36/U\_RAMB36

of frag REGCLKAU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[6].u\_

ramb36/U\_RAMB36\_REGCLKAU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[6].u\_

ramb36/U\_RAMB36

of frag REGCLKAL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[6].u\_

ramb36/U\_RAMB36\_REGCLKAL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[6].u\_

ramb36/U\_RAMB36

of frag REGCLKBU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[6].u\_

ramb36/U\_RAMB36\_REGCLKBU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[6].u\_

ramb36/U\_RAMB36

of frag REGCLKBL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[6].u\_

ramb36/U\_RAMB36\_REGCLKBL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[7].u\_

ramb36/U\_RAMB36

of frag REGCLKAU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[7].u\_

ramb36/U\_RAMB36\_REGCLKAU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[7].u\_

ramb36/U\_RAMB36

of frag REGCLKAL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[7].u\_

ramb36/U\_RAMB36\_REGCLKAL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[7].u\_

ramb36/U\_RAMB36

of frag REGCLKBU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[7].u\_

ramb36/U\_RAMB36\_REGCLKBU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[7].u\_

ramb36/U\_RAMB36

of frag REGCLKBL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[7].u\_

ramb36/U\_RAMB36\_REGCLKBL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[8].u\_

ramb36/U\_RAMB36

of frag REGCLKAU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[8].u\_

ramb36/U\_RAMB36\_REGCLKAU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[8].u\_

ramb36/U\_RAMB36

of frag REGCLKAL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[8].u\_

ramb36/U\_RAMB36\_REGCLKAL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[8].u\_

ramb36/U\_RAMB36

of frag REGCLKBU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[8].u\_

ramb36/U\_RAMB36\_REGCLKBU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[8].u\_

ramb36/U\_RAMB36

of frag REGCLKBL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[8].u\_

ramb36/U\_RAMB36\_REGCLKBL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[9].u\_

ramb36/U\_RAMB36

of frag REGCLKAU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[9].u\_

ramb36/U\_RAMB36\_REGCLKAU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[9].u\_

ramb36/U\_RAMB36

of frag REGCLKAL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[9].u\_

ramb36/U\_RAMB36\_REGCLKAL\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[9].u\_

ramb36/U\_RAMB36

of frag REGCLKBU connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[9].u\_

ramb36/U\_RAMB36\_REGCLKBU\_tiesig

WARNING:Pack:2874 - Trimming timing constraints from pin

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[9].u\_

ramb36/U\_RAMB36

of frag REGCLKBL connected to power/ground net

U\_ila\_pro\_0/U0/I\_YES\_D.U\_ILA/U\_CAPSTOR/I\_CASE1.I\_YES\_TB.U\_TRACE\_BUFFER/U\_RAM/

I\_V5.U\_CS\_BRAM\_CASCADE\_V5/I\_DEPTH\_LTEQ\_32K.U\_SBRAM\_0/I\_B36KGT0.G\_RAMB36[9].u\_

ramb36/U\_RAMB36\_REGCLKBL\_tiesig

Running directed packing...

Running delay-based LUT packing...

Updating timing models...

INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report

(.mrp).

Running timing-driven placement...

Total REAL time at the beginning of Placer: 10 secs

Total CPU time at the beginning of Placer: 9 secs

Phase 1.1 Initial Placement Analysis

Phase 1.1 Initial Placement Analysis (Checksum:f3d80433) REAL time: 11 secs

Phase 2.7 Design Feasibility Check

INFO:Place:834 - Only a subset of IOs are locked. Out of 9 IOs, 8 are locked and

1 are not locked. If you would like to print the names of these IOs, please

set the environment variable XIL\_PAR\_DESIGN\_CHECK\_VERBOSE to 1.

Phase 2.7 Design Feasibility Check (Checksum:f3d80433) REAL time: 11 secs

Phase 3.31 Local Placement Optimization

Phase 3.31 Local Placement Optimization (Checksum:903d67c3) REAL time: 11 secs

Phase 4.37 Local Placement Optimization

Phase 4.37 Local Placement Optimization (Checksum:903d67c3) REAL time: 11 secs

Phase 5.33 Local Placement Optimization

Phase 5.33 Local Placement Optimization (Checksum:903d67c3) REAL time: 19 secs

Phase 6.32 Local Placement Optimization

Phase 6.32 Local Placement Optimization (Checksum:903d67c3) REAL time: 19 secs

Phase 7.2 Initial Clock and IO Placement

.......

Phase 7.2 Initial Clock and IO Placement (Checksum:1770b0da) REAL time: 19 secs

Phase 8.36 Local Placement Optimization

Phase 8.36 Local Placement Optimization (Checksum:1770b0da) REAL time: 19 secs

Phase 9.30 Global Clock Region Assignment

Phase 9.30 Global Clock Region Assignment (Checksum:1770b0da) REAL time: 19 secs

Phase 10.3 Local Placement Optimization

.....

Phase 10.3 Local Placement Optimization (Checksum:fc084342) REAL time: 19 secs

Phase 11.5 Local Placement Optimization

Phase 11.5 Local Placement Optimization (Checksum:fc084342) REAL time: 19 secs

Phase 12.8 Global Placement

...................................................................................................................................................

.......

Phase 12.8 Global Placement (Checksum:f67bbf6f) REAL time: 21 secs

Phase 13.29 Local Placement Optimization

Phase 13.29 Local Placement Optimization (Checksum:f67bbf6f) REAL time: 21 secs

Phase 14.5 Local Placement Optimization

Phase 14.5 Local Placement Optimization (Checksum:f67bbf6f) REAL time: 21 secs

Phase 15.18 Placement Optimization

Phase 15.18 Placement Optimization (Checksum:9cab665e) REAL time: 29 secs

Phase 16.5 Local Placement Optimization

Phase 16.5 Local Placement Optimization (Checksum:9cab665e) REAL time: 29 secs

Phase 17.34 Placement Validation

Phase 17.34 Placement Validation (Checksum:9cab665e) REAL time: 29 secs

Total REAL time to Placer completion: 29 secs

Total CPU time to Placer completion: 28 secs

Running post-placement packing...

Writing output files...

Design Summary:

Number of errors: 0

Number of warnings: 46

Slice Logic Utilization:

Number of Slice Registers: 1,912 out of 19,200 9%

Number used as Flip Flops: 1,911

Number used as Latches: 1

Number of Slice LUTs: 2,221 out of 19,200 11%

Number used as logic: 2,027 out of 19,200 10%

Number using O6 output only: 1,555

Number using O5 output only: 333

Number using O5 and O6: 139

Number used as Memory: 169 out of 5,120 3%

Number used as Shift Register: 169

Number using O6 output only: 167

Number using O5 output only: 1

Number using O5 and O6: 1

Number used as exclusive route-thru: 25

Number of route-thrus: 364

Number using O6 output only: 358

Number using O5 output only: 6

Slice Logic Distribution:

Number of occupied Slices: 1,054 out of 4,800 21%

Number of LUT Flip Flop pairs used: 2,869

Number with an unused Flip Flop: 957 out of 2,869 33%

Number with an unused LUT: 648 out of 2,869 22%

Number of fully used LUT-FF pairs: 1,264 out of 2,869 44%

Number of unique control sets: 174

Number of slice register sites lost

to control set restrictions: 362 out of 19,200 1%

A LUT Flip Flop pair for this architecture represents one LUT paired with

one Flip Flop within a slice. A control set is a unique combination of

clock, reset, set, and enable signals for a registered element.

The Slice Logic Distribution report is not meaningful if the design is

over-mapped for a non-slice resource or if Placement fails.

OVERMAPPING of BRAM resources should be ignored if the design is

over-mapped for a non-BRAM resource or if placement fails.

IO Utilization:

Number of bonded IOBs: 9 out of 172 5%

Number of LOCed IOBs: 8 out of 9 88%

Number of bonded IPADs: 6

Number of LOCed IPADs: 6 out of 6 100%

Number of bonded OPADs: 4

Number of LOCed OPADs: 4 out of 4 100%

Specific Feature Utilization:

Number of BlockRAM/FIFO: 17 out of 36 47%

Number using BlockRAM only: 17

Total primitives used:

Number of 36k BlockRAM used: 11

Number of 18k BlockRAM used: 9

Total Memory used (KB): 558 out of 1,296 43%

Number of BUFG/BUFGCTRLs: 4 out of 32 12%

Number used as BUFGs: 4

Number of BSCANs: 1 out of 4 25%

Number of BUFDSs: 1 out of 4 25%

Number of LOCed BUFDSs: 1 out of 1 100%

Number of GTP\_DUALs: 1 out of 2 50%

Number of LOCed GTP\_DUALs: 1 out of 1 100%

Number of PLL\_ADVs: 1 out of 2 50%

Number of STARTUPs: 1 out of 1 100%

Number of TEMACs: 1 out of 2 50%

Number of RPM macros: 9

Average Fanout of Non-Clock Nets: 3.62

Peak Memory Usage: 528 MB

Total REAL time to MAP completion: 31 secs

Total CPU time to MAP completion: 30 secs

Mapping completed.

See MAP report file "topMain\_map.mrp" for details.

Process "Map" completed successfully

Started : "Place & Route".

Running par...

Command Line: par -w -intstyle ise -ol high -mt off topMain\_map.ncd topMain.ncd topMain.pcf

Constraints file: topMain.pcf.

Loading device for application Rf\_Device from file '5vlx30t.nph' in environment C:\Xilinx\13.3\ISE\_DS\ISE\.

"topMain" is an NCD, version 3.2, device xc5vlx30t, package ff323, speed -1

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)

Initializing voltage to 0.950 Volts. (default - Range: 0.950 to 1.050 Volts)

Device speed data version: "PRODUCTION 1.73 2011-10-03".

Device Utilization Summary:

Number of BSCANs 1 out of 4 25%

Number of BUFDSs 1 out of 4 25%

Number of LOCed BUFDSs 1 out of 1 100%

Number of BUFGs 4 out of 32 12%

Number of GTP\_DUALs 1 out of 2 50%

Number of LOCed GTP\_DUALs 1 out of 1 100%

Number of External IOBs 9 out of 172 5%

Number of LOCed IOBs 8 out of 9 88%

Number of External IPADs 6 out of 186 3%

Number of LOCed IPADs 6 out of 6 100%

Number of External OPADs 4 out of 8 50%

Number of LOCed OPADs 4 out of 4 100%

Number of PLL\_ADVs 1 out of 2 50%

Number of RAMB18X2s 6 out of 36 16%

Number of RAMB36\_EXPs 11 out of 36 30%

Number of STARTUPs 1 out of 1 100%

Number of TEMACs 1 out of 2 50%

Number of Slices 1054 out of 4800 21%

Number of Slice Registers 1912 out of 19200 9%

Number used as Flip Flops 1911

Number used as Latches 1

Number used as LatchThrus 0

Number of Slice LUTS 2221 out of 19200 11%

Number of Slice LUT-Flip Flop pairs 2869 out of 19200 14%

Overall effort level (-ol): High

Router effort level (-rl): High

INFO:Timing:3386 - Intersecting Constraints found and resolved. For more information, see the TSI report. Please

consult the Xilinx Command Line Tools User Guide for information on generating a TSI report.

Starting initial Timing Analysis. REAL time: 5 secs

Finished initial Timing Analysis. REAL time: 5 secs

Starting Router

Phase 1 : 14143 unrouted; REAL time: 6 secs

Phase 2 : 11325 unrouted; REAL time: 6 secs

Phase 3 : 3432 unrouted; REAL time: 11 secs

Phase 4 : 3432 unrouted; (Setup:0, Hold:8837, Component Switching Limit:0) REAL time: 12 secs

Updating file: topMain.ncd with current fully routed design.

Phase 5 : 0 unrouted; (Setup:0, Hold:8614, Component Switching Limit:0) REAL time: 14 secs

Phase 6 : 0 unrouted; (Setup:0, Hold:8614, Component Switching Limit:0) REAL time: 14 secs

Phase 7 : 0 unrouted; (Setup:0, Hold:8614, Component Switching Limit:0) REAL time: 14 secs

Phase 8 : 0 unrouted; (Setup:0, Hold:8614, Component Switching Limit:0) REAL time: 14 secs

Phase 9 : 0 unrouted; (Setup:0, Hold:0, Component Switching Limit:0) REAL time: 14 secs

Phase 10 : 0 unrouted; (Setup:0, Hold:0, Component Switching Limit:0) REAL time: 15 secs

Total REAL time to Router completion: 15 secs

Total CPU time to Router completion: 15 secs

Partition Implementation Status

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No Partitions were found in this design.

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Generating "PAR" statistics.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Generating Clock Report

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

+---------------------+--------------+------+------+------------+-------------+

| Clock Net | Resource |Locked|Fanout|Net Skew(ns)|Max Delay(ns)|

+---------------------+--------------+------+------+------------+-------------+

| clk25m | BUFGCTRL\_X0Y1| No | 305 | 0.373 | 1.871 |

+---------------------+--------------+------+------+------------+-------------+

| clk125m |BUFGCTRL\_X0Y31| No | 445 | 0.423 | 1.934 |

+---------------------+--------------+------+------+------------+-------------+

| icon\_control0<0> |BUFGCTRL\_X0Y30| No | 81 | 0.360 | 1.871 |

+---------------------+--------------+------+------+------------+-------------+

|U\_icon\_pro/U0/iUPDAT | | | | | |

| E\_OUT | Local| | 1 | 0.000 | 0.519 |

+---------------------+--------------+------+------+------------+-------------+

| icon\_control0<13> | Local| | 5 | 0.000 | 0.778 |

+---------------------+--------------+------+------+------------+-------------+

\* Net Skew is the difference between the minimum and maximum routing

only delays for the net. Note this is different from Clock Skew which

is reported in TRCE timing report. Clock Skew is the difference between

the minimum and maximum path delays which includes logic delays.

\* The fanout is the number of component pins not the individual BEL loads,

for example SLICE loads not FF loads.

Timing Score: 0 (Setup: 0, Hold: 0, Component Switching Limit: 0)

Number of Timing Constraints that were not applied: 4

Asterisk (\*) preceding a constraint indicates it was not met.

This may be due to a setup or hold violation.

----------------------------------------------------------------------------------------------------------

Constraint | Check | Worst Case | Best Case | Timing | Timing

| | Slack | Achievable | Errors | Score

----------------------------------------------------------------------------------------------------------

TS\_MGTREFCLKP = PERIOD TIMEGRP "MGTREFCLK | SETUP | 1.130ns| 6.870ns| 0| 0

P" 8 ns HIGH 50% INPUT\_JITTER 0.5 ns | HOLD | 0.241ns| | 0| 0

----------------------------------------------------------------------------------------------------------

TS\_XLXN\_33\_0 = PERIOD TIMEGRP "XLXN\_33\_0" | SETUP | 2.084ns| 29.580ns| 0| 0

TS\_MGTREFCLKP / 0.2 HIGH 50% INP | HOLD | 0.336ns| | 0| 0

UT\_JITTER 0.5 ns | | | | |

----------------------------------------------------------------------------------------------------------

TS\_MGTREFCLKN = PERIOD TIMEGRP "MGTREFCLK | MINLOWPULSE | 3.999ns| 4.000ns| 0| 0

N" 8 ns HIGH 50% INPUT\_JITTER 0.5 ns | | | | |

----------------------------------------------------------------------------------------------------------

TS\_U\_TO\_J = MAXDELAY FROM TIMEGRP "U\_CLK" | SETUP | 12.174ns| 2.826ns| 0| 0

TO TIMEGRP "J\_CLK" 15 ns | HOLD | 1.418ns| | 0| 0

----------------------------------------------------------------------------------------------------------

TS\_U\_TO\_U = MAXDELAY FROM TIMEGRP "U\_CLK" | SETUP | 14.120ns| 0.880ns| 0| 0

TO TIMEGRP "U\_CLK" 15 ns | HOLD | 0.557ns| | 0| 0

----------------------------------------------------------------------------------------------------------

TS\_J\_CLK = PERIOD TIMEGRP "J\_CLK" 30 ns H | SETUP | 21.263ns| 8.737ns| 0| 0

IGH 50% | HOLD | 0.465ns| | 0| 0

----------------------------------------------------------------------------------------------------------

TS\_XLXN\_33 = PERIOD TIMEGRP "XLXN\_33" TS\_ | MINPERIOD | 37.778ns| 2.222ns| 0| 0

MGTREFCLKN / 0.2 HIGH 50% INPUT\_J | | | | |

ITTER 0.5 ns | | | | |

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PATH "TS\_D2\_TO\_T2\_path" TIG | SETUP | N/A| 2.756ns| N/A| 0

----------------------------------------------------------------------------------------------------------

PATH "TS\_J2\_TO\_D2\_path" TIG | N/A | N/A| N/A| N/A| N/A

----------------------------------------------------------------------------------------------------------

PATH "TS\_J3\_TO\_D2\_path" TIG | N/A | N/A| N/A| N/A| N/A

----------------------------------------------------------------------------------------------------------

PATH "TS\_J4\_TO\_D2\_path" TIG | MAXDELAY | N/A| 3.127ns| N/A| 0

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PATH "TS\_J\_TO\_D\_path" TIG | SETUP | N/A| 3.761ns| N/A| 0

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PATH "TS\_D\_TO\_J\_path" TIG | SETUP | N/A| 3.589ns| N/A| 0

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Derived Constraint Report

Review Timing Report for more details on the following derived constraints.

To create a Timing Report, run "trce -v 12 -fastpaths -o design\_timing\_report design.ncd design.pcf"

or "Run Timing Analysis" from Timing Analyzer (timingan).

Derived Constraints for TS\_MGTREFCLKN

+-------------------------------+-------------+-------------+-------------+-------------+-------------+-------------+-------------+

| | Period | Actual Period | Timing Errors | Paths Analyzed |

| Constraint | Requirement |-------------+-------------|-------------+-------------|-------------+-------------|

| | | Direct | Derivative | Direct | Derivative | Direct | Derivative |

+-------------------------------+-------------+-------------+-------------+-------------+-------------+-------------+-------------+

|TS\_MGTREFCLKN | 8.000ns| 4.000ns| 0.444ns| 0| 0| 0| 0|

| TS\_XLXN\_33 | 40.000ns| 2.222ns| N/A| 0| 0| 0| 0|

+-------------------------------+-------------+-------------+-------------+-------------+-------------+-------------+-------------+

Derived Constraints for TS\_MGTREFCLKP

+-------------------------------+-------------+-------------+-------------+-------------+-------------+-------------+-------------+

| | Period | Actual Period | Timing Errors | Paths Analyzed |

| Constraint | Requirement |-------------+-------------|-------------+-------------|-------------+-------------|

| | | Direct | Derivative | Direct | Derivative | Direct | Derivative |

+-------------------------------+-------------+-------------+-------------+-------------+-------------+-------------+-------------+

|TS\_MGTREFCLKP | 8.000ns| 6.870ns| 5.916ns| 0| 0| 23635| 25580|

| TS\_XLXN\_33\_0 | 40.000ns| 29.580ns| N/A| 0| 0| 25580| 0|

+-------------------------------+-------------+-------------+-------------+-------------+-------------+-------------+-------------+

All constraints were met.

INFO:Timing:2761 - N/A entries in the Constraints List may indicate that the

constraint is not analyzed due to the following: No paths covered by this

constraint; Other constraints intersect with this constraint; or This

constraint was disabled by a Path Tracing Control. Please run the Timespec

Interaction Report (TSI) via command line (trce tsi) or Timing Analyzer GUI.

Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 15 secs

Total CPU time to PAR completion: 15 secs

Peak Memory Usage: 462 MB

Placer: Placement generated during map.

Routing: Completed - No errors found.

Timing: Completed - No errors found.

Number of error messages: 0

Number of warning messages: 0

Number of info messages: 1

Writing design to file topMain.ncd

PAR done!

Process "Place & Route" completed successfully

Started : "Generate Post-Place & Route Static Timing".

Running trce...

Command Line: trce -intstyle ise -v 3 -s 1 -n 3 -fastpaths -xml topMain.twx topMain.ncd -o topMain.twr topMain.pcf -ucf topmain.ucf

Loading device for application Rf\_Device from file '5vlx30t.nph' in environment

C:\Xilinx\13.3\ISE\_DS\ISE\.

"topMain" is an NCD, version 3.2, device xc5vlx30t, package ff323, speed -1

Analysis completed Thu Dec 21 08:40:09 2017

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Generating Report ...

Number of warnings: 0

Total time: 6 secs

Process "Generate Post-Place & Route Static Timing" completed successfully

Started : "Generate Programming File".

Running bitgen...

Command Line: bitgen -intstyle ise -f topMain.ut topMain.ncd

INFO:Bitgen:40 - Replacing "Auto" with "NoWait" for option "Match\_cycle". Most

commonly, bitgen has determined and will use a specific value instead of the

generic command-line value of "Auto". Alternately, this message appears if

the same option is specified multiple times on the command-line. In this

case, the option listed last will be used.

WARNING:PhysDesignRules:1841 - One or more GTPs are being used in this design.

Evaluate the SelectIO-To-GTP Crosstalk section of the Virtex-5 RocketIO GTP

Transceiver User Guide to ensure that the design SelectIO usage meets the

guidelines to minimize the impact on GTP performance.

WARNING:PhysDesignRules:372 - Gated clock. Clock net icon\_control0<13> is

sourced by a combinatorial pin. This is not good design practice. Use the CE

pin to control the loading of data into the flip-flop.

Process "Generate Programming File" completed successfully